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Estimation of interface state density of Si(100)/MgO interface for spin injection into Silicon

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Abstract

Si(100)/MgO/Ta MOS devices were fabricated for estimating interface trap states density (D_{it}) in the Si(100)/MgO interface. We fabricated MgO films by RF magnetron sputtering and EB evaporation methods. The influence of post annealing and thin Mg layer insertion on crystal structure, surface roughness, and interface states density were investigated. As a results, we have observed least trap density ($D_{it} \sim 4\times10^{12}$ cm^{-2}eV^{-1}) for samples with MgO films deposited by the EB evaporation without post annealing.

1. Introduction

Spin transports between two ferromagnetic (FM) electrodes through semiconductor (SC) have been demonstrated by many groups using local/non-local Hanle and spin-valve measurements. However, the observed intensity of three terminal spin signals were larger than the value from standard spin diffusion theory, and non-local spin signals were considerably smaller than predicted value from spin polarization of FM electrodes. The mechanism of spin transport in real FM/Insulator/SC junction is not well understood.

Jansen *et al*. proposed a model which consider direct tunneling and two-step tunneling via interface states in parallel and spin signal will be a weighted average of spin accumulation in channel and interface state [1]. The effect of localized defects in the tunnel barrier for three terminal Hanle signal was experimentally proved by inelastic tunneling spectroscopy, however, it was concluded that confined interface states rather contributes spin signal amplification [2]. From the viewpoint of highly polarized spin injection, Si(100)/MgO structure is promising because some Co-based Heusler alloys grown on MgO(100) constitutes *B*2-ordered structure [3] which shows half-metallicity. Moreover, MgO(100) tunnel barrier can induce coherent tunneling effect through the Δ_1 band of MgO and widely used for magnetic tunnel junctions. However, the interface states at Si/MgO prevent high-efficient spin injection into Silicon.

In this work, we prepared Si(100)/MgO/Ta MOS capacitors with RF magnetron sputtering and EB evaporation methods and investigated the effect of post annealing and insertion of thin Mg layer of crystal structure, surface roughness, and interface trap state density for the high efficient spin injection into silicon.

2. Experiment

The films were deposited on p-type Si(100) wafers using ultrahigh vacuum magnetron sputtering and EB evaporation system ($P_{base} < 3.0\times10^{-6}$ Pa). The carrier density of Si substrate was 8.1×10^{17} cm^{-3}. Before loading in the chamber, all the substrates were cleaned ultrasonically in semicoclean23 (Furuuchi Chemical Co.) for 20 minutes, dipped 1% HF for 3 min, and ultra-pure water for 1 min. Then, the substrates were introduced in the chamber immediately, and flushed at 650°C for 10 min. The stacking structure of MOS capacitors were Si/ sputtered-MgO(20)/ Ta(10), Si/ sputtered-Mg(0.8)/ sputtered-MgO(19.2)/ Ta(10), and Si/ EB-evaporated- MgO(20)/ Ta(10) (in nm). Ar pressure for all sputtering films was 0.1 Pa. The growth rate of EB evaporation MgO was ca. 0.60 Å/sec. Both samples with and without post annealing were fabricated. The post annealing process was performed after the deposition of MgO films at 300°C for 10 min *in situ*. The MOS capacitor devices were fabricated using photolithography and argon ion milling methods. The shape of MOS capacitors was circle and the diameters were 400 μm. The crystal structure, surface roughness, and high frequency capacitance-voltage characteristics at room temperature were measured by out-of-plane/in-plane x-ray diffractometer (XRD), atomic force microscope (AFM) and LCR meter (Agilent E4980A), respectively.

3. Results and Discussion

Fig. 1(a) shows the out-of-plane XRD patterns (2θ-θ profile) of Si(100)/MgO/Ta structures. As can be seen, the MgO (200) peaks were clearly observed around $2\theta = 43°$ with sputtered-MgO and Mg/MgO samples. It indicates 001-oriented MgO films were obtained on Si(100) substrate. Among of them, the samples with post annealing process demonstrated smaller FWHM of rocking curves around the 200 peaks (not shown here). On the other hand, MgO (111) peaks were observed in EB evaporation samples. Fig. 1(b) shows the in-plane XRD patterns ($2\theta\chi/\varphi$ profile) of the samples. Contrary to the out of plane scan, there was no MgO (200) peak in all samples. It implies that all the samples had polycrystalline structure along in-plane direction. Fig. 2 illustrates surface roughness (R_a) as a function of annealing temperature. The value of R_a slightly increased as annealing temperature increased in all the samples. This feature might be come from MgO crystallization. EB evaporated MgO films had more flat surface than sputtered MgO films and lowest value was R_a =

0.20 nm without post annealing.

The high frequency capacitance-voltage (CV) curves of Si(100)/MgO/Ta MOS capacitors measured at room temperature was shown in Fig. 3. The black line is the ideal CV curve calculated for same doping density and MgO thickness without interface traps [4]. The stretch out of experimental CV curves along gate voltage is corresponded to the interface traps occupancy change. Fig. 4 shows the interface traps density (D_{it}) versus gate voltage estimated from high frequency CV curves. The Mg inserted samples showed larger D_{it} value than samples without Mg insertion, and it indicates that Mg atoms were not completely oxidized and the un-oxidized MgO formed trapping states. The EB evaporated MgO sample without annealing formed least trap state as ~4×10^{12} $cm^{-2}eV^{-1}$ under the conduction band. It is indicated that MgO tunneling barrier prepared by EB evaporation is greatly useful to decrease interface states in Si(100)/MgO/Ferro-magnets spin injection devices.

4. Summary

Si(100)/MgO/Ta MOS capacitors were fabricated with RF magnetron sputtering and EB evaporation methods. The sputtered MgO and thin Mg layer inserted samples showed 001-orientation on Si substrates. We concluded that EB evaporation method without post annealing is promising for reduction of interfacial trap states at Si(100)/MgO interface to realize high-efficient spin injection into Si.

Acknowledgements

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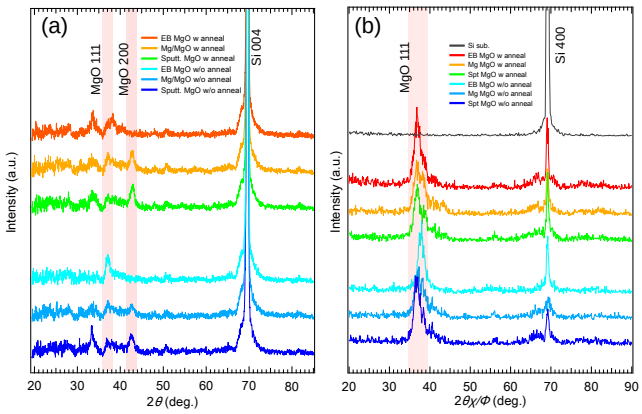

Fig. 1 (a) Out of plane (2θ-θ) and (b) in-plane ($2\theta\chi$/φ) XRD patterns of Si(100)/MgO/Ta structures.

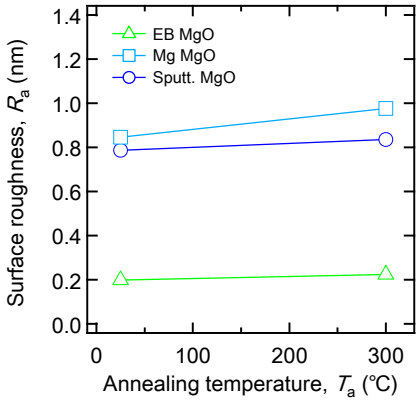

Fig. 2 Annealing temperature dependence of surface roughness (R_a) of Si(100)/MgO/Ta MOS structures.

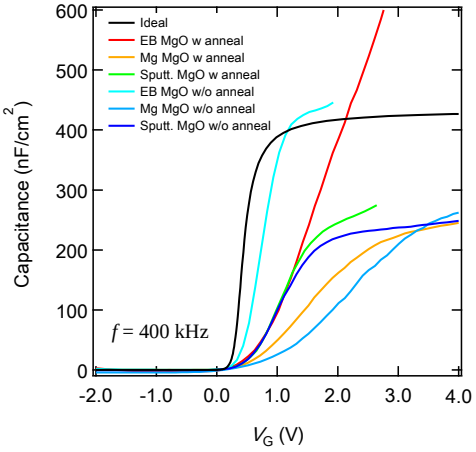

Fig. 3 High frequency capacitance-voltage curves of Si(100)/MgO/Ta MOS capacitors.

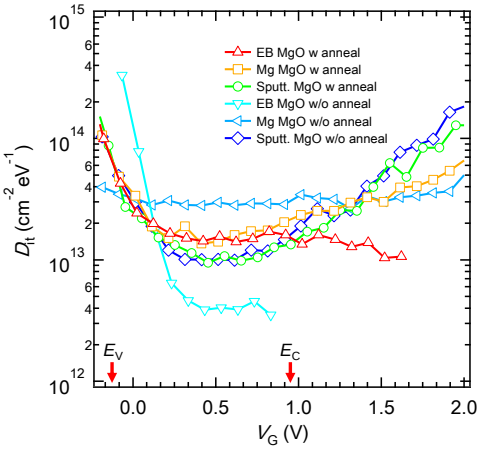

Fig. 4 Gate voltage dependence of interface states density (D_{it}) of Si(100)/MgO/Ta MOS capacitors.