Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp1301-1302

A New Compact Model for Accurate RF Noise Simulation in Sub-40nm nMOSFETs

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Abstract

A new compact model has been developed for accurate RF noise simulation and extraction of the actual intrinsic noise in sub-40 nm multi-finger nMOSFETs. This model can predict and verify the excess noise sources before and after deembedding, the mechanism responsible for the complicated layout dependence in various noise parameters, and facilitate low noise design in nanoscale CMOS technology.

I. Introduction

The aggressive gate length (L_g) scaling to sub-40nm in CMOS devices can raise the ideal intrinsic f_T to near THz (10^{12}Hz) [1]. However, the actual intrinsic f_T is far below THz due to the impact from the intrinsic parasitic RC, which cannot be eliminated by existing deembedding methods [2]-[5]. For the multi-finger (MF) MOSFETs widely used in RF circuits for gate resistance (R_g) reduction, the gate sidewall and finger-end fringing capacitances (C_{of} and $C_{f(poly\text{-}end)}$), and source resistances (R_S) appear as the primary factors limiting f_T and f_{MAX} [4]-[6]. Furthermore, the complicated trade-off between R_g, R_S, and $C_{f(poly\text{-}end)}$ brings critical impact on the RF noise parameters, such as NF_{min}, R_n, $Re(Y_{opt})$, and $Im(Y_{opt})$. Unfortunately, the mentioned effects were not taken into the conventional compact models like BSIM-4, which is widely used for logic circuits simulation but inadequate for RF simulation. In general, BSIM-4 simulation using the default thermal noise model always leads to severe under-estimation of the RF noise [7]. Moreover, the intrinsic noise extraction by using conventional noise correlation matrix method reveals abnormal fluctuation in the noise parameters [8], which makes it difficult to identify the layout dependent effects. The aforementioned challenges motivate our interest of this paper to explore a new compact model with proven accuracy in high frequency performance and RF noise simulation for sub-40nm nMOSFETs.

II. MF Devices Fabrication and Characterization

Fig.1(a)~(d) illustrate MF nMOSFETs and openM1 deembedding structures fabricated in 65nm HP CMOS process. As shown in Fig.2, the intrinsic device parameters like L_g, $T_{ox(inv)}$, and ΔW (due to STI top corner rounding) required for simulation can be determined by our proprietary method [9]. For this work using 65nm HP process, the results are L_g=37.5nm, $T_{ox(inv)}$=2.06nm, and ΔW=69.2nm. More importantly, the 3-D fringing capacitances from the gate sidewall and finger-end to source/drain diffusion and contacts, denoted as $C_{g,Diff}$, $C_{g,CT}$ (C_{of}=$C_{g,Diff}$+$C_{g,CT}$), and $C_{f(poly\text{-}end)}$ appear as intrinsic parasitic capacitances with critical impact on f_T, f_{MAX}, and RF noise but cannot be extracted and removed, even using openM1 deembedding down to the bottom metal (M1). Raphael simulation is an effective way to calculate $C_{g,Diff}$, $C_{g,CT}$, and $C_{f(poly\text{-}end)}$, and the accuracy can be verified by a comparison with the intrinsic gate capacitances, such as $C_{ggg,DUT}$ and $C_{gd,DUT}$ after openM1 deembedding.

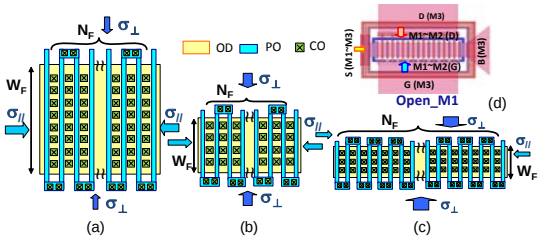

Fig. 1 MF MOSFETs layout with W_FxN_F=32μm (a) W2N16 (b) W025N128 (c) W0125N256 (d) openM1 deembedding structure. OD : active region, PO : poly-gate, CO : contacts.

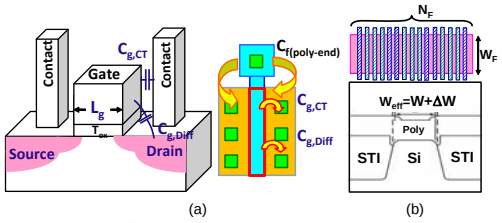

Fig.2 (a) Schematics of MOSFET with L_g, $T_{ox(inv)}$, gate sidewall fringing capacitance C_{of}=$C_{g,Diff}$ +$C_{g,CT}$ and finger-end fringing capacitance $C_{f(poly\text{-}end)}$ (b) MF MOSFET cross section showing ΔW due to STI TCR and W_{eff}.

III. High frequency and RF noise measurement - verification of BISM-4 simulation

High frequency S-parameters and RF noise parameters were measured by using Keysight PNA system (50GHz) and ATN NP5B system (18GHz), respectively. Fig.3(a) and (b) present the intrinsic gate capacitances $C_{gg,DUT}$ and $C_{gd,DUT}$ after openM1 deembedding (symbols) given by (1) and a comparison with BSIM-4 simulation using default and modified C-V models. Apparently, the default C-V model reveals severe under-estimation of $C_{gg,DUT}$ and $C_{gd,DUT}$ and it reflects the problem of neglecting intrinsic parasitic capacitances like C_{of} and $C_{f(poly\text{-}end)}$. As for the modified C-V model by adding the intrinsic parasitic capacitances in terms of $C_{gs,fr}$ and $C_{gd,fr}$ originated from C_{of} and $C_{f(poly\text{-}end)}$ given by (2), the simulation can reach a good agreement with the measurement. The significant increase of $C_{gg,DUT}$ and $C_{gd,DUT}$ when increasing N_F indicate that $C_{gs,fr}$ and $C_{gd,fr}$ may dominate the intrinsic channel capacitance in case of very large N_F due to $C_{f(poly\text{-}end)}$xN_F, according to (2). As for RF noise of our special focus, BSIM-4 simulation using default MOSFET model again exposes severe under-estimation of all noise parameters, such as NF_{min}, R_n, $Re(Y_{opt})$, and $|Im(Y_{opt})|$ as shown in Fig.4.

$$C_{gg,DUT} = \left.\frac{\mathrm{Im}(Y_{11,int})}{\omega}\right|_{(\omega R_g C_{gg})^2 \ll 1},\quad C_{gd,DUT} = \left.\frac{-\mathrm{Im}(Y_{12,int})}{\omega}\right|_{(\omega R_g C_{gg})^2 \ll 1} \qquad (1)$$

$$C_{gs,fr} + C_{gd,fr} = C_{of}\cdot W_{tot} + C_{f(poly-end)}\cdot N_F \qquad (2)$$

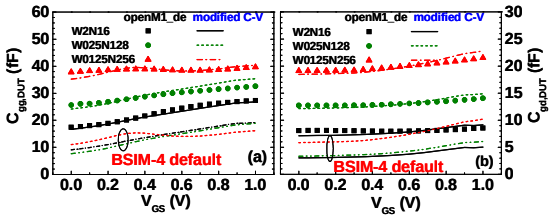

Fig.3 Intrinsic gate capacitances achieved by openM1 deembedding (symbols) and BSIM-4 simulation using default and modified C-V models (a) $C_{gg,DUT}$ vs. V_{GS} (b) $C_{gd,DUT}$ vs. V_{GS} for MF nMOSFETs at V_{DS}=1.0V.

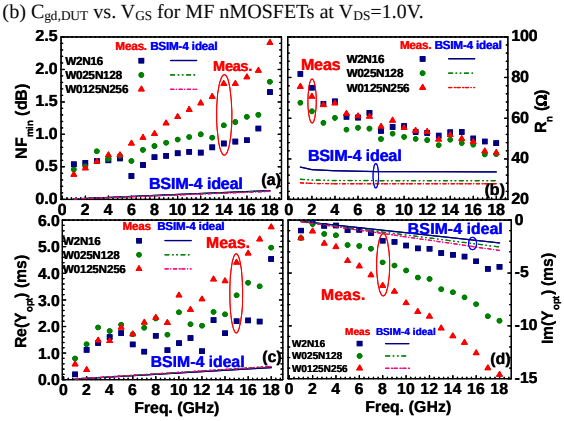

Fig.4 Noise parameters by measurement (symbols) and BSIM-4 simulation

(lines) using ideal MOSFET model for MF nMOSFETs at V_{DS}=1.0V, V_{GS}=0.7V (a) NF_{min} (b) R_n (c) $Re(Y_{opt})$ (d) $Im(Y_{opt})$.

IV. A New Compact Model for Accurate HF Parameters and RF Noise Simulation

The first step to solve aforementioned problems is an improved MOSFET model developed as shown in Fig.5 consisting of an ideal intrinsic MOSFET, intrinsic parasitic RLC, and a body RC network model. Herein, $C_{gs,fr}$ and $C_{gd,fr}$ represent the intrinsic parasitic capacitances containing C_{of} and $C_{f(poly-end)}$. The accuracy of this improved MOSFET model has been proven by a good match with the intrinsic Y-parameters, shown in Fig.6.

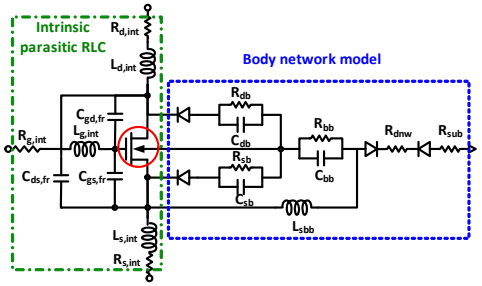

Fig.5 The improved MOSFET model including an ideal intrinsic MOSFET (red circle), intrinsic parasitic RLC (green dash-dot box), and a body network model (blue dash box).

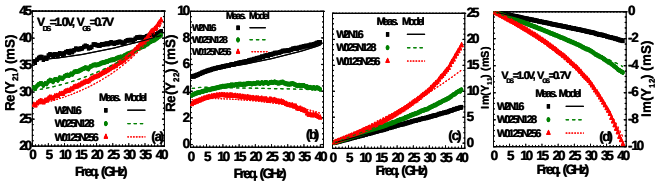

Fig. 6 Comparison of intrinsic Y-parameters after openM1 deembedding and simulation using improved MOSFET model (a) $Re(Y_{21})$ (b) $Re(Y_{22})$ (c) $Im(Y_{11})$ and (d) $Im(Y_{12})$ for MF nMOSFETs at V_{DS}=1.0V, V_{GS}=0.7V.

Taking the improved MOSFET model as the base, a full equivalent circuit model (not shown for brevity) can be established by adding a lossy substrate RLC network [10] for accurate simulation of the impact from the pads, interconnection lines, and lossy substrate on high frequency characteristics and RF noise prior to deembedding. The accuracy of this full equivalent circuit model has been validated by a good match with the measured Y-parameters before deembedding (not shown). However, even with proven accuracy in Y-parameters, the RF noise simulation by BSIM-4 using default thermal noise model (dash lines) shown in Fig. 7 reveals significant deviation from the measurement (symbols), such as severe under-estimation of R_n for all three MF nMOSFETs, under-estimated NF_{min} but over-estimated $Re(Y_{opt})$ for W0125N256. The only way to reduce this deviation is to make a significant change to the thermal noise model parameters in BSIM-4 [7] given by (3)-(4) in which β_{tnoi} and θ_{tnoi} are fitting parameters to reach required tuning of R_n and $Re(Y_{opt})$. As shown in Fig.7, the simulation by modified thermal noise parameter (solid lines) can reach much better fitting to the measurement.

This new compact model can accurately predict the RF noise prior to deembedding and explain the mechanism responsible for the abnormal layout dependence, such as minor difference of R_n, but significant increase of $Re(Y_{opt})$ and NF_{min} when increasing N_F. The increase of $Re(Y_{opt})$ is originated from the increase of $Im(Y_{11})$ due to $C_{gs,fr}$ and $C_{gd,fr}$ given by (2) and extrinsic parasitic capacitances from the stacked metals, interconnect, and pads calculated by the lossy substrate model [10]. The minor difference of R_n can be understood from the analytical model given by (5) in which the smaller R_g realized by larger N_F is offset by the larger g_{do}/g_m^2 due to lower g_m from larger R_S. The combined effect of $Re(Y_{opt})$ and R_n leads to the increase of NF_{min} when increasing N_F. It means that the smaller R_g achieved by larger N_F and smaller W_F cannot guarantee the smaller R_n.

As shown in Fig. 8, the actual intrinsic RF noise (symbols) can be calculated by the improved MOSFTE model **(**Fig.5) and indicate significant reduction of NF_{min}, $Re(Y_{opt})$, and $|Im(Y_{opt})|$ compared with the extrinsic noise **(**Fig.7**)**, due to elimination of excess noise from the lossy substrate RLC. For W0125N256 with the worst extrinsic noise, the intrinsic NF_{min} at 18GHz is around 0.58dB, which is 1.54 dB reduction from the extrinsic NF_{min} of 2.12dB, attributed to the significant decrease of $Re(Y_{opt})$. In comparison, the ideal MOSFET model free from any parasitic RLC reveals abnormally small intrinsic noise (lines), such as NF_{min} below 0.14dB at18GHz, but actually it cannot be achieved by real devices even after a truly clean deembedding.

$$\beta_{tnoi} = RNOIA \cdot \left[1 + TNOIA \cdot L_{eff} \cdot \left(V_{gsteff} / E_{sat} L_{eff}\right)^2\right] \quad (3)$$

$$\theta_{tnoi} = RNOIB \cdot \left[1 + TNOIB \cdot L_{eff} \cdot \left(V_{gsteff} / E_{sat} L_{eff}\right)^2\right] \quad (4) \qquad R_n = R_g + \gamma(\omega)\left(\frac{g_{do}}{g_m^2}\right) \quad (5)$$

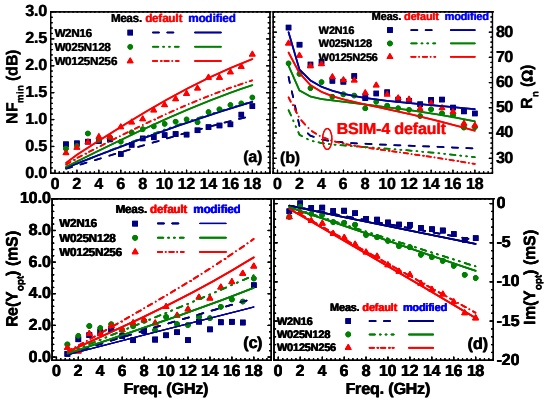

Fig. 7 Comparison of measured noise parameters and BSIM-4 simulation using default (dash lines) and modified (solid lines) thermal noise model in a full equivalent circuit (a) NF_{min} (b) R_n (c) $Re(Y_{opt})$ and (d) $Im(Y_{opt})$ for multi-finger nMOSFET at V_{DS}=1.0V, V_{GS}=0.7V.

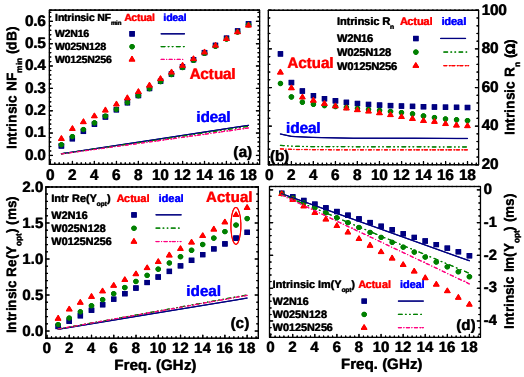

Fig.8 Intrinsic noise parameters by BSIM-4 simulation using ideal intrinsic (line) and improved MOSFET model (symbols) and modified thermal noise model for ideal and actual intrinsic MOSFETs (a) NF_{min} (b) R_n (c) $Re(Y_{opt})$ (d) $Im(Y_{opt})$ for multi-finger nMOS at V_{DS}=1.0V, V_{GS}=0.7V

V. Conclusion

A new compact model developed in this paper can accurately simulated RF noise and analyze the excess noise sources. The effective way to suppressing NF_{min} should resort to $Re(Y_{opt})$ and R_n reduction by elimination of extrinsic parasitic RLC via a truly clean deembedding and minimization of intrinsic parasitic RC like R_g, R_S, C_{of} and $C_{f(poly-end)}$, via multi-finger device layout optimization, low resistivity conductors for gate electrode as well as interconnect, and low-k dielectric for gate sidewall spacer.

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