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Ring VCO based ultra low jitter PLL architecture

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***Abstract*— This paper describes a fully integrated Semi-Digital PLL (SDPLL) design based on pseudo-differential ring VCO with extremely low jitter using a 122.88MHz input. The SDPLL achieves low jitter using a very high loop bandwidth to reduce the noise contribution from the VCO through the loop transfer function. To achieve that, new charge pump architecture with sample and hold technique is introduced.**

I. INTRODUCTION

PLLs are widely used for clock generation in different electronic circuit and systems. To achieve low jitter, LC VCOs are used in state of the art PLLs. Ring VCOs use only a fraction of the area and the power compared to high performance LC oscillators, but are ~20dBc/Hz worse in Phase Noise performance.

To filter the high ring oscillator phase noise, an aggressive noise shaping through the loop transfer function is required. The PLL acts as a high pass filter for the VCO. The loop bandwidth is limited by the update frequency of the PLL, which is 245.76 MHz in this implementation (using a frequency Doubler). Pushing the PLL bandwidth as close as possible to the PFD update frequency, VCO`s phase noise is attenuated aggressively to achieve low jitter. Hence it is very important to consider the discrete nature of the loop. To achieve this, the SDPLL is modelled in z-domain instead of using the s-domain approximation.

To circumvent the drawback of having higher switching transients due to higher loop bandwidth, which results in higher reference spur, Sample and Hold technique is introduced to mask these transients to the VCO.

II. SDPLL ARCHITECTURE

The standard architecture of a SDPLL is shown in figure 1. The proportional and integral control paths are separated there. Circuits used for reference current (Ref. Current) block, storage cells and the phase frequency detector (PFD) are the same as in [1] and [2] i.e. the integral path is unchanged.

A complete new proportional path is implemented in this work and is discussed in detail.

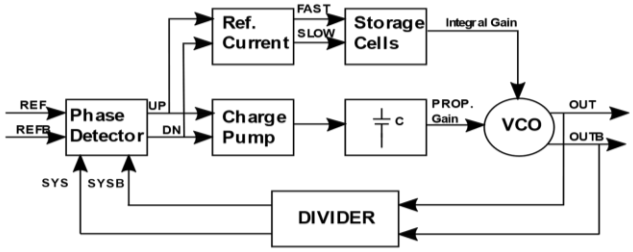

Figure 1: SDPLL Block Diagram

A. Proportional Charge Pump Circuit

The charge pump circuit is shown in figure 2. When a UP pulse comes from PFD, the CP dumps the charge on the capacitor proportional to the UP pulse width through M1. When DOWN (DN) pulse comes, the charge is depleted proportional to DOWN pulse width through M2. In other words charge stored or depleted is proportional to the instantaneous phase difference between Reference (REF) and Feedback (SYS) signals. At the end of each update cycle Capacitor C1 is always pulled back by transistors M3, M4, M5 and M6 to the voltage, at which UP and DOWN currents cancel. So the capacitor acts as a memory-less element, just like a resistor to supply the proportional control voltage in traditional PLL.

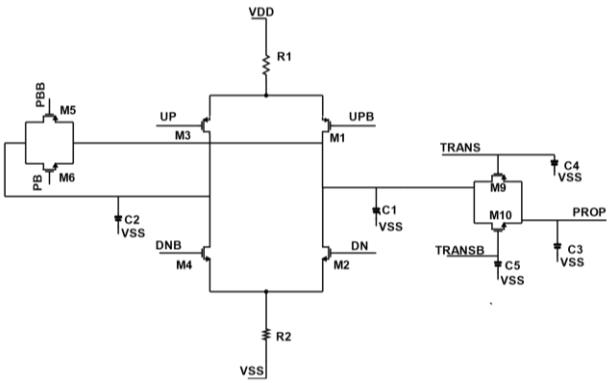

Figure 2: Charge Pump and LPF capacitor

Pull Back (PB/PBB) is coupled to the sampling signal (TRANS) unlike [1] and [2]. Further details of PB signal have been discussed in conjunction with TRANS in section III.

III. SAMPLING IMPLEMENTATION AND EFFECTS

The control voltage switching transients create spurs at the output of the VCO. In case of integral control voltage, the transients are negligible (in microvolt range) but on the proportional control voltage they are significant.

The voltage from the capacitor C1 of the proportional voltage is sampled after a short delay to avoid these spikes and in this way the update effect is masked for the VCO. A classic sample and hold circuit is used as shown in the figure 3.

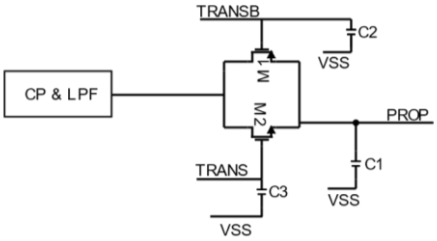

Figure 3 : Sample & Hold circuit implementation

The sampling signal TRANS & TRANSB is generated every falling edge of the UP signal as shown in the figure 4.

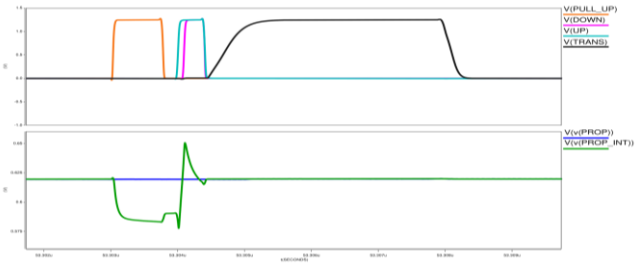

Fig 4: UP, DOWN, PULL_UP, PROP_INT and PROP

The falling edge of the TRANS signal completes the sampling, thus is used to pull back (PB) or pull up the internal PROP voltage (before the transfer gate) to its nominal value. Compared to [1] and [2] in this scheme PROP is active for the full period, hence bandwidth is increased.

IV. Test Results

This architecture was implemented for two cases, one with a low noise input path and a jitter of 336fs was achieved, as shown in the figure 5.

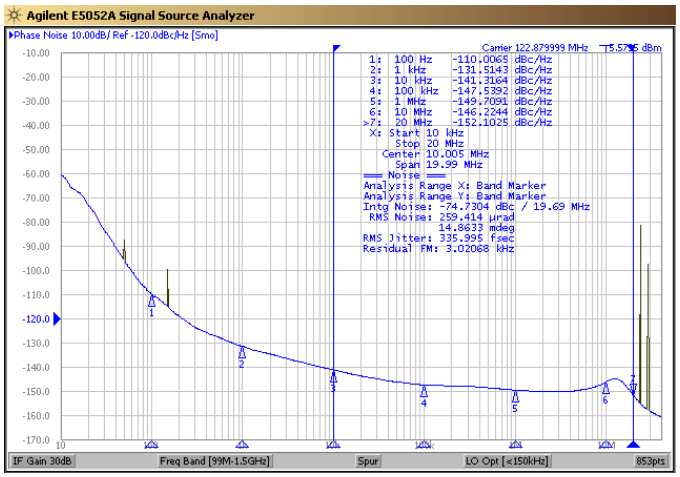

Figure 5 : Jitter and Phase Noise measurement results

In the 2nd implementation input had higher jitter. Higher Bandwidth was achieved, resulting in 240fs jitter as shown in figure 6.

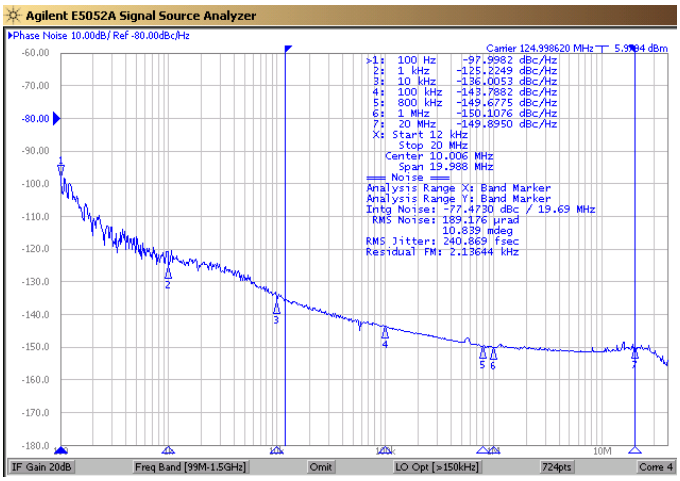

Figure 6 : Jitter and Phase Noise measurement results

V1. Conclusion

The RMS. jitter is lower than the recently published work. In-band phase noise performance of this SDPLL is very good. From 100Hz to 100kHz the phase noise is even better than state of the art LC VCO based PLLs. Table 1 compares the proposed PLL to the state of the art.

Table 1

	This Work	[2]	[3]	[4]
f_{VCO}	1.3GHz	400 MHz	Not Specified	3.1 GHz
f_{ref}	122.88 MHz	50 MHz	40MHz – 350MHz	108MHz
Tuning Range	100MHz-2GHz	0.2 GHz – 0.4GHz	0.4GHz – 1.4GHz	1.4GHz – 3.2GHz
RMS Jitter	336 fs / 240 fs	0.7 ps	1.7 ps	1.01 ps
Power	35mW	29mW	0.78mW	27.5mW
FOM	-233 dB	-228 dB	-237 dB	-226 dB
VDD	2.4 V	3.3 V	0.8 V	1.2 V
Area	0.16 mm^2	0.11 mm^2	0.007mm^2	0.32 mm^2
Process	130 nm	0.4 µm	65 nm	65 nm

V11. REFERENCES

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