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Experimental study of bias stress degradation of organic thin film transistors

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***Abstract*—The dependence of bias stress voltage on device performance degradation of an organic thin film transistor (OTFT) is discussed. The test chip measurement results show that the gate voltage affects more significantly on the short term device degradation than drain current flow. The measurement results also indicate that the degradation recovers partially once the given bias voltage is removed. We propose a set of equations that represent the model parameter degradation and its recovery. Finally, we fit the proposed model to the measurement results.**

1. Background

Organic thin film transistors (OTFTs) can be fabricated on flexible and relatively large materials through printing process. Taking advantage of that property, they are expected to be used wherein silicon devices are difficult to apply. OTFTs, however, have relatively short lifetime [1], hence the modeling of their performance degradation is the topic of intensive researches [2-5].

In this paper, we focus on bias stress degradation of OTFTs. The gate electric field and the drain current flow are considered as the major contributors of bias stress degradation. However, quantitative measurement result has not yet been reported. Knowing the dominant factor is significantly important in modeling bias stress degradation. Through a test chip fabrication, we compare temporal degradation of OTFTs under different bias conditions. We also propose a set of degradation model for device model parameters, which considers current recovery observed after removing the stress voltages.

2. Measurement setup

Our target device is a top-contact and bottom-gate OTFT, whose layer stack is shown in Fig. 1(a) [6]. In the layout design of the test chip, four OTFTs are grouped as a set, over which stress application and the current measurements are conducted simultaneously. In order to facilitate the parallel measurement, a 12-pin DC probe is used. Each probe needle is connected to individual source measure unit (SMU). The channel length and the width of the OTFT are $50\,\mu\mathrm{m}$ and $1000\,\mu$m, respectively.

We firstly measure I_D-V_GS curves, which takes approximately 17 seconds, and then different stress conditions listed in Fig. 3 are applied for 30 seconds to each transistor. This measurement-stress period is repeated for 30 times. The condition "none" applies no stress bias to the OTFT, while the condition "Vgs" applies gate voltage only and "Vgs+Vds" applies both gate and drain bias voltages. In "Vgs/none" condition, the "Vgs" and "none" are alternatively repeated. Here, in the "Vgs+Vds" condition, the drain current flows continuously during the stress period. The stress voltage V_stress is $-3\,\mathrm{V}$ or $-4\,\mathrm{V}$. The measurements are carried out on six p-type OTFT sets. The following discussions are on a representative set.

3. Measurement results and modeling

Fig. 4 shows the change of $I_\mathrm{D}-V_\mathrm{GS}$ curve for the OTFT with "Vgs" stress condition with $V_\mathrm{stress}=-4\,\mathrm{V}$. With the repetitive application of the stress bias voltage, mobility as well as threshold voltage keeps shifting. Fig. 5 shows the temporal I_D degadation for $V_\mathrm{stress}=-3\,\mathrm{V}$ and $-4\,\mathrm{V}$. The saturation currents at $V_\mathrm{GS}=V_\mathrm{DS}=-3.0\,\mathrm{V}$ are presented. The current degradation of the transistors under "Vgs" condition is larger than that in "Vgs+Vds." This result suggests that the gate potential is the dominant degradation source for OTFT. The drain voltage in the "Vgs+Vds" condition reduces effective gate potential due to the voltage slope developed along the channel length.

In Fig. 5(b), I_D recovers clearly when bias stress is removed, as seen in "Vgs/none" condition. We hence propose a following degradation model for two device parameters, V_th and carrier mobility (μ):

$$\Delta p(t+t_0) = \Delta_1+\Delta_2, \tag{1}$$

$$\Delta_1 = \phi\left(1-\exp\left(-At^n\right)\right), \tag{2}$$

$$\Delta_2 = \Delta p(t_0)\left(1-\left(\frac{1-\exp\left[-Bt\right]}{1-\exp\left[-B\left(t+t_0\right)\right]}\right)^m\right). \tag{3}$$

Here, p is a model parameter; V_th or μ in this paper. A, B, ϕ, and m, n are the fitting parameters and t_0 is the reference time wherein devices are fresh. As opposed to the conventional model [4], our model incorporates a recovery term in Eq. (3). By assuming the degradation is caused by the similar mechanism as in the carrier trapping-detrapping model [7] used for modeling bias temperature instability of silicon transistors. Fig. 6 shows extracted degradation of V_th and μ, with their fitting result. The model equation expresses the recovery in "Vgs/none" condition. Including the stress voltage and drain voltage dependence into the proposed model, and the fitting for long-term degradation are our future work.

4. Conclusion

In this work, we experimentally studied bias stress induced degradation of OTFTs. On the basis of the measurement results, we proposed a model parameter degradation model for the simulation of temporal degradation of circuit performance. The experimental results demonstrate that the proposed model well reproduces the degradation and recovery.

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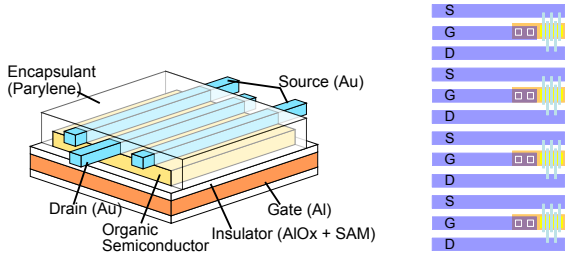
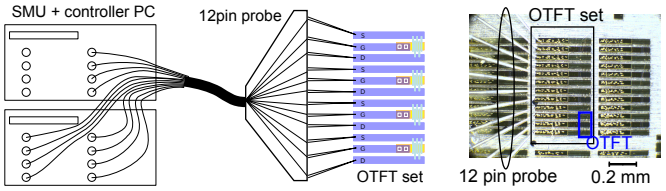


(a) OTFT device structure (b) Layout design

Fig. 1: Transistor structure and the layout of a OTFT set. Four independent OTFTs in an OTFT set are measured in a parallel manner using a 12-pin DC probe. Probing pads of the OTFT set are drawn long to improve endurance against repetitive probing.



(a) Conceptual diagram of the measurement (b) Microphotograph

Fig. 2: Parallel Kervin measurement of four OTFTs in a OTFT set. Bias voltage application and current measurements are automated by controller PC. (a) Each terminal is independently controlled by respective SMU channel. (b) The OTFT set under probing.

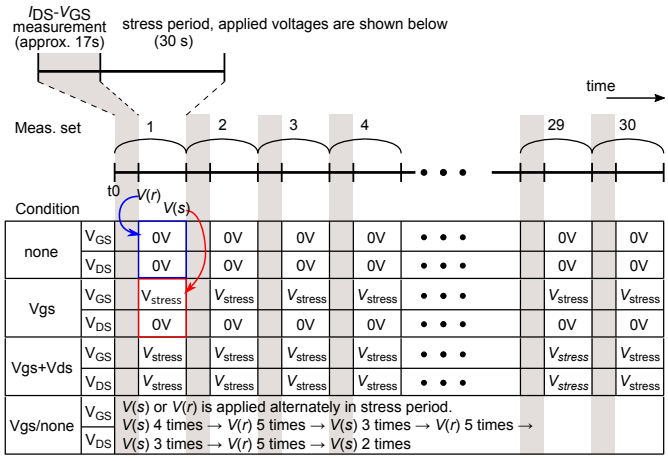


Fig. 3: Measurement sequences for four stress conditions. A set of I-V curve measurement and stress application, which take approximately 17 s and 30 s, are repeated for 30 times. "Vgs/none" apply "Vgs" stress condition ($V(s)$; $V_{\mathrm{GS}} = V_{\mathrm{stress}}$, $V_{\mathrm{DS}} = 0.0\,\mathrm{V}$) and "none" condition ($V(r)$; $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 0.0\,\mathrm{V}$) alternatively.

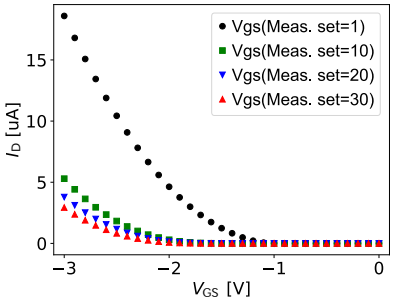
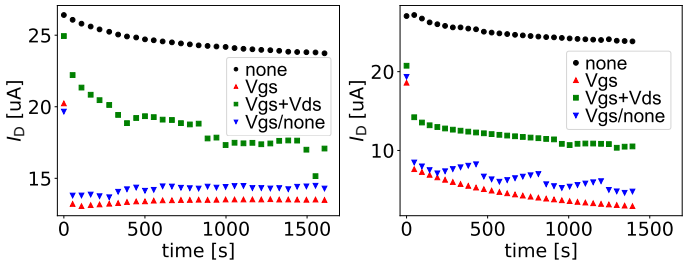
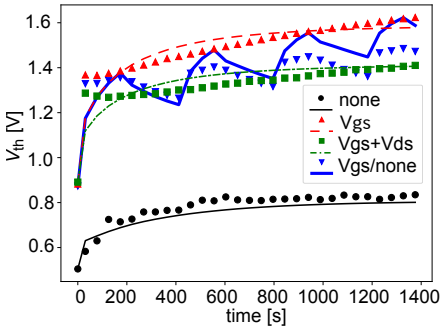


Fig. 4: Measured I-V curves in the "Vgs" stress condition at $V_{\mathrm{stress}} = -4.0\,\mathrm{V}$. Both the x-intercept and the slope of the curves change as total stress period becomes longer. This observation suggests degradation models are necessary for both threshold voltage and carrier mobility shift.

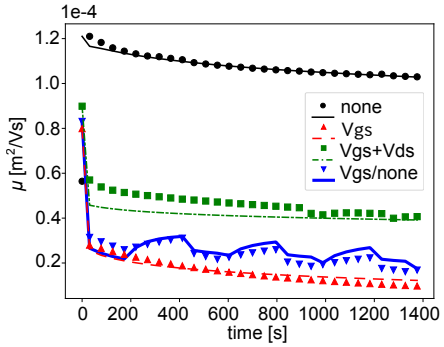


(a) $V_{\mathrm{stress}} = 3.0\,\mathrm{V}$ (b) $V_{\mathrm{stress}} = 4.0\,\mathrm{V}$

Fig. 5: Measured drain currents at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = -3.0\,\mathrm{V}$. Larger degradation has been observed in (b) than that in (a). The trend of current recovery is clearer in the alternative stress condition (Vgs/none).



(a) Threshold voltage



(b) Mobility

Fig. 6: Extracted threshold voltages and carrier mobility during the measurement of Fig. 5-(b) are shown as symbols. The fitting results using the proposed model are also plotted with lines.