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Monolithically Integrated Optical OR Gate Using Light-Emitting Transistors

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Abstract

We develop an optical OR gate circuit including Light-Emitting Transistors (LET) and Heterojunction Phototransistors (HPT) on GaAs substrate by the monolithically integrated fabrication. Because the OR gate has the characteristic of dual input and output of the optical signal and the electrical signal, it can transmit the information more quickly and take advantage of Opto-Electrical Integrated Circuits (OEICs) effectively.

1. Introduction

With the advancement of technology nowadays, the improvement of data transmission speed becomes more important. In order to satisfy the demands of logic units and memory storage, the achievement of OEICs turns into the trend in the semiconductor fabrication field.

LET was invented in 2004 by Milton Feng and Nick Holonyak [1], it was a heterojunction bipolar transistor which has a quantum well in the base region. When the electrons diffuse through the base region, they may be captured by the quantum well and recombined with the holes, forming the optical output [2]. Another device named HPT, can absorb light by the base/collector junction, turning the optical signal to the electrical signal by Franz–Keldysh effect [3]. The two devices mentioned above are both the "three-ports" devices that can deal with the input and output of the optical signal and the electrical signal.

We use LET and HPT in our circuit design, fabricating the OR gate by the monolithically integrated method. And we prove that the optical logic gates are usable in Opto-Electronic Integrated systems through practical fabrication process and measurement.

2. General Instructions

Device Structure and Fabrication Process

We simplify the fabrication process by adopting the monolithically integrated fabrication method. Starting with the definition of base and collector mesa, we use the sulfuric acid and hydrogen peroxide aqueous solution to do the wet etching process. Second, the E-gun evaporator is used to make the metal electrodes, the p-type electrode metal is Ti/Pt/Au and n-type is Au/Ge/Ni/Au. And the isolation etching process is for structure protection. As for the back-end fabrication, we coat the polyimide passivation layer and etch the via hole. Finally, the Ni-Cr resistance is deposited and the fabrication process is finished.

Fig.1 illustrates the cross-section structure of HPT and LET. HPT as the light absorption component, the size of its emitter is 20*40 μm^2, and the diameter of the emitter is 80 μm for LET. The OR gate circuit design and the OM image of the device are in Fig.2.

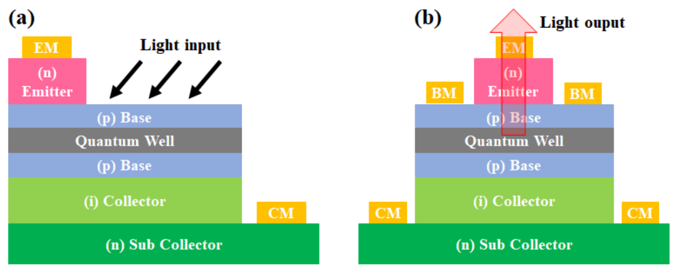

Fig. 1 The cross-section structure imaging of (a) HPT and (b) LET.

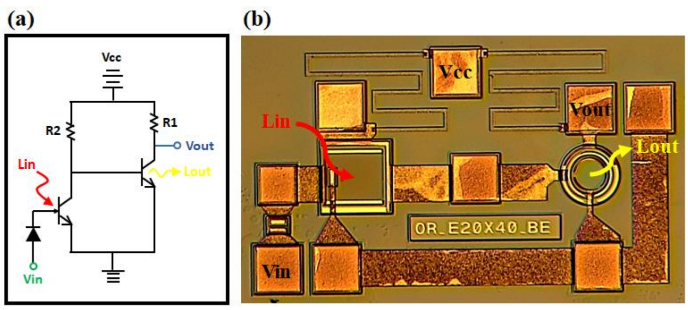

Fig. 2 (a) the OR gate circuit and (b) OR gate OM imaging.

Measurement Results

We use the precision IV analyzer and the DC probe tips for the electrical measurement of the OR gate. A laser diode coupled with fiber is applied as the input light source, and the light output of the OR gate is measured by a photodetector. Fig.3 shows the I-V curve of the HPT under different power of input light. And the electrical family curve and output curve of LET is in Fig.4, the load line is defined to choose the operation point.

Fig.5 is the logic measurement results of the OR gate. The voltage value was 3V for Vcc. Vin is also 3V and the frequency is 1kHz, inputting by square wave format with a time interval. The light input (Lin) power is 2.5mW and the power is 2kHz. The actual measurement data is shown in Table 1.

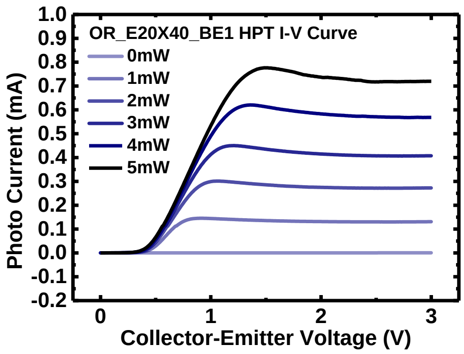

Fig. 3 HPT I-V curve under different power of input light.

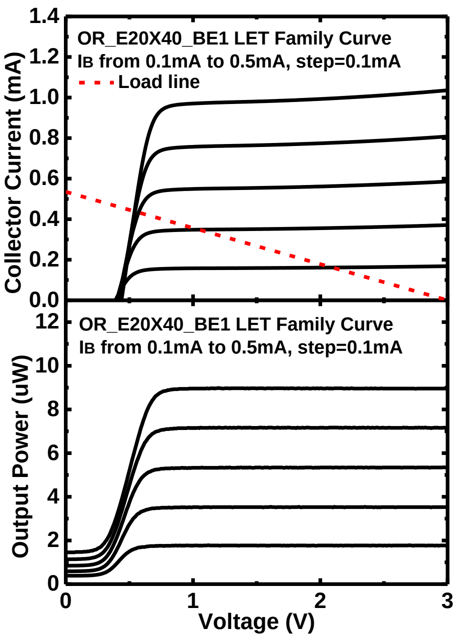

Fig. 4 The electrical family curve and output curve of LET.

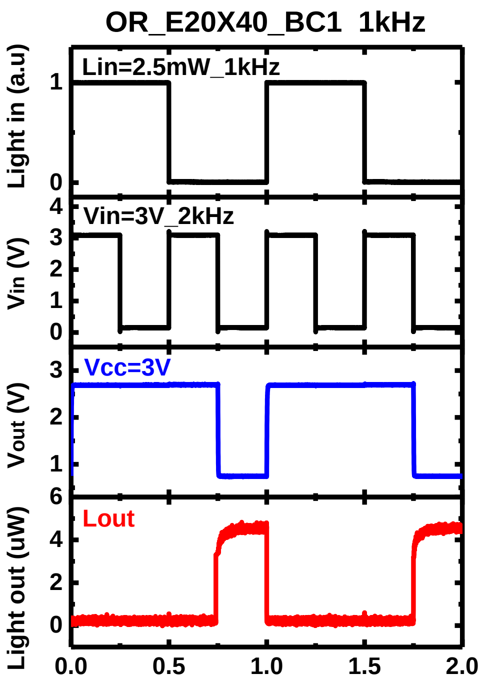

Fig. 5 OR gate logic measurement results.

Table 1

Vcc = 3V						
Input				Output		
Lin		Vin		Vout		Lout
State	Power (mW)	State	Voltage (V)	State	Voltage (V)	State
1	2.5	1	3	1	2.69	0
1	2.5	0	0	1	2.69	0
0	0	1	3	1	2.69	0
0	0	0	0	0	0.73	1

According to the measurement results, when the HPT has one of the optical input or the electrical input (or both), it will turn on. And the current will not flow to the base of the LET, so the LET fails to turn on. There is no voltage drop between two sides of the resistance R1. The output voltage (Vout) is state 1 and the light output (Lout) is state 0. Only when the HPT doesn't have optical or electrical input, it will not turn on and the current will flow to the base of the LET and make it turn on. The light output is state 1 and the voltage output is state 0 because of the voltage drop between two sides of R1. So this circuit provide an electrical OR gate and an optical NOR gate.

3. Conclusions

Base on the logic measurement results in Fig.5, we successfully fabricated an optical OR gate including LET and HPT components by the monolithically integrated method. Different designs of the circuit can also be used to create different optical logic gates, which have both optical and electrical signal output. In addition, using the optical signal to transmit information has a faster modulation speed than using the electrical signal, so it has advantages in fulfilling the requirement of massive data transmission. We also hope to expand the application area of OEICs by combining multiple logic gates to form more complex circuits, like SR latches, flip-flops, and others.

Acknowledgements

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References

[1] Feng, M., N. Holonyak Jr, and W. Hafez. "Light-emitting transistor: Light emission from InGaP/GaAs heterojunction bipolar transistors." Applied physics letters 84.1 (2004): 151-153.

[2] Feng, M., N. Holonyak Jr, and R. Chan. "Quantum-well-base heterojunction bipolar light-emitting transistor." Applied physics letters 84.11 (2004): 1952-1954.

[3] Sasaki, Akio, and Masaaki Kuzuhara. "InGaAsP-InP heterojunction phototransistors and light amplifiers." Japanese Journal of Applied Physics 20.4 (1981): L283..