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Evaluation of Multi-stage, Unileg, Si-nanowire Thermoelectric Generator with A Cavity-free and Planar Device Architecture

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Abstract

We demonstrate a multi-staged thermoelectric generator (TEG) for high voltage using Si-nanowires (Si-NWs) with a cavity-free planar architecture. The fabricated TEG, which is so-called unileg-TEG, comprises only n-type Si-NWs. The fabrication process of the unileg TEG is simple compared with bileg-TEGs which composed of a series connection of n- and p-type thermoelectric materials. The results shows that the output voltage of the unileg-TEG is successfully enhanced by increasing the number of the TEG stages. Although unileg-TEGs have an intrinsic drawback due to the direct connection between cold-side electrodes and the hot-side electrodes of neighboring TEG elements, its adverse effect can be compensated by increasing the areal density of the TEGs.

1. Introduction

Thermoelectric (TE) energy harvesters which utilize environmental heat energies are anticipated for the portable, wearable or swarmed sensor nodes in internet of things (IoT) systems. In previous works, we demonstrated that a single-stage cavity-free planar TE generator (TEG) using sub-μm class short Si-NWs generated a high areal density of output power [1-3]. The next target is the multi-stage integration of the proposed TEG, where a large number of TEG elements is connected in series to elevate the output voltage to about hundreds mV, which is necessary to drive a DC/DC boost converter supplying enough voltages for wireless transmitters, sensors, and other load devices.

TEGs are categorized into two groups: unileg- and bileg-TEGs. A unileg-TEG is composed only n-type or p-type semiconductors, so that it is suitable for the first trial of the integration of our proposed TEG architecture. However, in the unileg-TEG, a cold-side electrode of the TEG element is wired in series to a hot-side electrode of neighboring TEG elements, as shown in Fig. 1. The inter-μTEG connecting wire conducts not only the electric current but also the heat current. Thus, the heat leakage, which is indicated the red arrow in Fig. 1, flows to the neighboring TEG cold-side electrode through the connecting wire, so that the temperature across the Si-NWs in each TEG is diminished. In this work, we experimentally and numerically investigate the stage-number dependence of the TE performance of the cavity-free planar unileg-TEG using n-type Si-NWs.

2. Structure of Si-NW TEG

The multi-stage planar TEG is fabricated on an SOI substrate, as shown schematically in Fig. 2. The thicknesses of the Si-substrate, the BOX SiO_2 layer, and the top SOI layer were 745 μm, 145 nm, and 50 nm, respectively. The SOI layer was patterned into Si-NWs with a width of less than 100 nm. Phosphorus ions (dose 5.0×10^{15} ions/cm^2) were implanted at an acceleration energy of 10 keV. The implantation was followed by activation annealing at 1000 °C. A single device comprised a 80-line Si-NW bundle with a pitch of 500 nm. The lengths of the Si-NWs (L_{NW}) are 0.25 and 1.00 μm. Both the ends of a Si-NW bundle were connected to separate Si pads. These Si-NWs and Si pads were wrapped in an SiO_2 interlayer insulator. Next, this SiO_2 layer at the Si pad regions was removed. A 400 nm-thick Al/TiN/Ti was deposited on the Si pad as the electrode. The hot side electrode of the TEG is connected in series to cold side of the other TEG by 2μm-width Al wire. The TEG stage-number is 3, 5, 7, 9, and 18.

The TE power was measured by externally applying a temperature difference ΔT_{ext} between surface and bottom of the specimen. The hot-side electrode was heated by attaching a micro-thermostat, whose temperature is maintained at 28 or 38 ºC. The base stage beneath the substrate was maintained at 23 ºC by a Peltier cooler. The heat current flowed perpendicularly to the Si substrate and partially exuded in the horizontal direction. The exuded heat current formed a steep temperature gradient in the proximity of the heat source, thereby inducing a TE current through the Si-NWs.

3. Results and Discussion

The electrical resistance, R, is proportionally increased by increasing the TEG stage-number (Fig.3a), and the R per one TEG is almost constant (Fig. 3b). The total open circuit voltage Voc is also increased, but it does not show a complete linear dependence on the stage-number (Fig.3c). Here we define an effective Seebeck coefficient as $Voc/\Delta T_{ext}$, where ΔT_{ext} is the externally applied temperature difference. The effective Seebeck coefficient per each TEG element is shown in Fig.3d, Although the data are largely scattered, it seems decreased as the stage-number increases. This is due to that the total heat current through the hot-side electrodes increases as the stage-number increases, thereby the temperature difference between hot-side and cold-side electrodes is decreased by the increase in the heat leakage current through the metal intra-connection.

The effect of the heat leakage can be compensated by increasing the areal density of the TEGs. To show this, we perform an FEM analysis by using COMSOL Multiphysics®. Fig. 4 depicts the unit cell of the simulated multi-stage TEG. The thermal conductivity parameters are summarized in Table I. In the simulation, the distance between the TEGs is varied to change the TEG density result shows that the effective Seebeck coefficient Voc per each TEG element decreases by decreasing the distance between the TEGs (Fig. 5a). This result indicates that the temperature difference applied between each TEG element decreases due to the increase in the thermal current density.

On the other hand, the areal power density of unileg-TEG

is increases by shrinking the interval between TEG elements (Fig. 5b). Thus, the effect of heat leakage in the unileg-TEG can be compensated by increasing the areal density of the TEGs. Considering the higher fabrication cost of bileg-TEG, high density unileg-TEG is a practical solution of the multi-staged, cavity-free, planar Si-NW TEG module.

4. Conclusions

We discussed the stage-number dependence of the TEG performance of the multi-stage unileg Si-NWs TEG with our proposed cavity-free planar device architecture. The effective Seebeck coefficient par elemental decreases with increasing the stage-number, because of the increase in the heat leakage current through the metal intra-connection in unileg-TEG module. However, fortunately, in our proposed device architecture, this effect is compensated by increasing the areal TEGs density.

Acknowledgements

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References

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Table I thermal conductivities and interfacial thermal resistance used in FEM simulation.

	κ (W/m·K)		$\theta_{interface}$ (K·m²/W)
Al	238	Al/AlN	15×10^{-9}
AlN	150	Al/Si	20×10^{-9}
SiO_2	1.4	Al/SiO_2	7×10^{-9}
Si-sub	131	AlN/SiO_2	10×10^{-9}
Si-NW	131	Si/SiO_2	2×10^{-9}

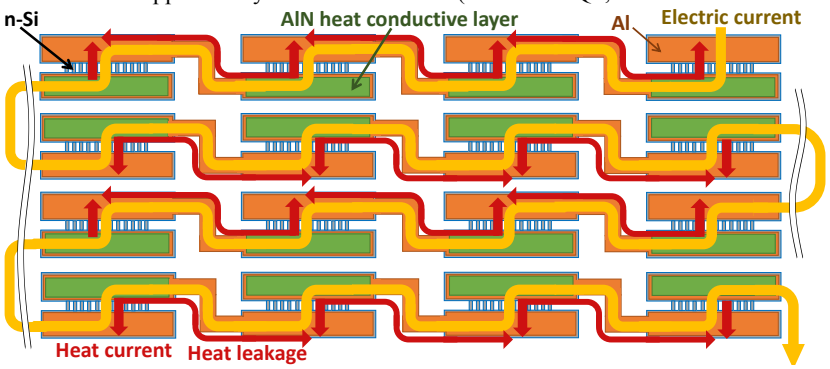

Fig 1 Schematic of unileg planar Si-NWs TE generator (top view).

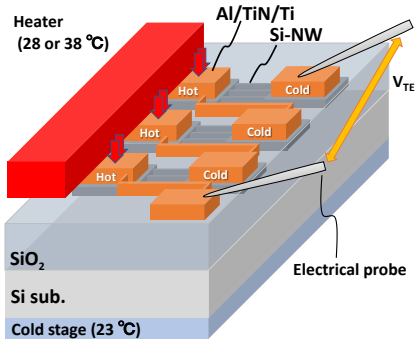

Fig. 2 Fabricated TE generator.

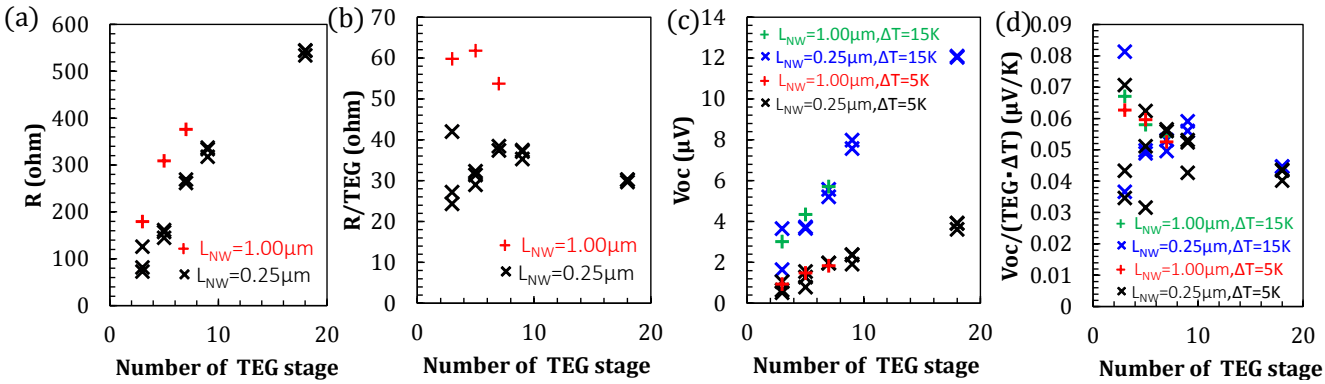

Fig 3 TEG stage-number dependency of (a) electrical resistance, R, (b) R per one TEG, (c) open circuit voltage, Voc, and (d) effective Seebeck coefficient per each TEG element.

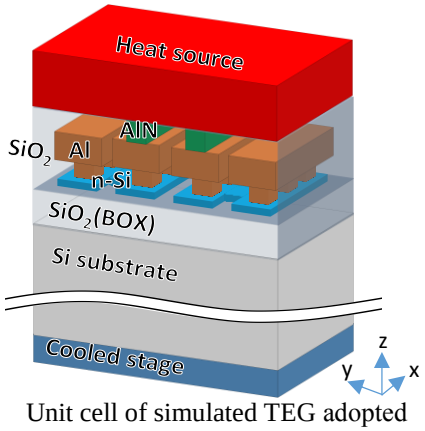

Fig 4 Unit cell of simulated TEG adopted periodic boundary condition in *xy* direction.

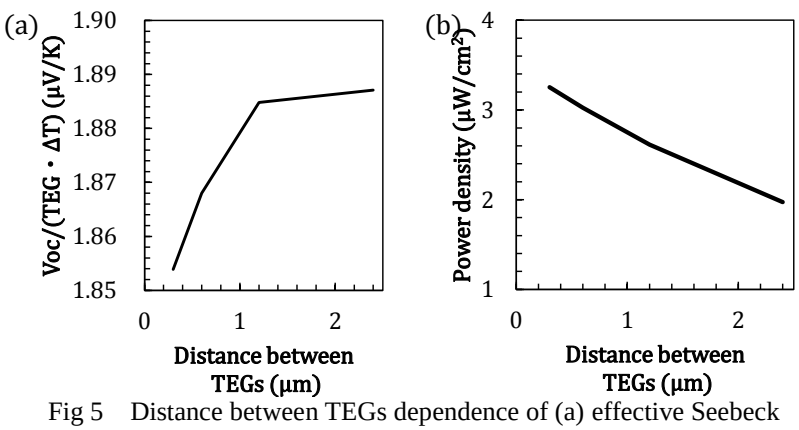

Fig 5 Distance between TEGs dependence of (a) effective Seebeck coefficient per each TEG element and (b) areal power density.