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Backend Engineering of Cavity-free Planar Si-nanowire Thermoelectric Generator

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Abstract

We perform a design optimization of the backend structure of a cavity-free planar micro TE generator (μ-TEG) using Si nanowires (Si-NWs). It is found that the heat injection from the heat source should be moderately restricted to maintain a low temperature of the cold-side electrode. By shrinking the footprint of the heat guide to the hot-side electrode, the output power density can be improved by 24%. The optimum backend structure makes more scalable the proposed μ-TEG.

1. Introduction

μ-TEG is attracting attention as a perpetual power source for distributed sensor nodes of IoT systems. Recently, silicon nanowires (Si-NWs) emerged as a promising thermoelectric material [1,2]. Since then, a number of fabrication examples of Si-based TEGs has been reported.

Our research group proposed a planar μ-TEG architecture without cavity structure on the SOI substrate (Fig.1) [3,4]. The key to an efficient operation is how the temperature difference across the Si-NW is maintained. To do so, the heat current must go through only a heat guide on the hot-side electrode [5], and the heat current toward the cold-side electrode must be prohibited by an interlayer. Thus, the backend structure determines the TE performance of the device. In this study, we perform a design optimization of the backend structure of the cavity-free planar μ-TEG.

2. Simulation method

Fig. 2 and 3 shows the structure of the top and cross-sectional view of the μ-TEG. The thicknesses of heater, AlN heat guide, Al-electrode, Al-contact, Si-NW, SiO_2 BOX layer, and Si substrate layer are 400 nm, 1 μm, 400 nm, 100 nm, 50 nm, 145 nm, and 50 μm, respectively. The length and width of the Si-NWs are 250 nm and 125 nm, respectively. The distance between the Si-NWs is 355 nm. Most part of the μ-TEG is designed with a $\lambda = 0.6$ μm rule. The contact area is $3\lambda \times 3\lambda$. The distance between neighboring Al-contacts, the margin width between Al-contacts, the edge of Si-Pad, and the interval between neighboring TEG elements are unified to λ. The thermal conductivity and interfacial thermal resistance parameters are shown in Table I. The finite element method simulation software COMSOL Multiphysics® was used for device simulation.

In this study, three different heat guide structures are considered: (Type A) Symmetric structure between hot- and cold-side electrodes, (Type B) the heat guide and hot-side electrode is shrunk with fixing the interval of the TEG elements, and (Type C) the interval between neighboring TEG elements is shrunk from that of Type B structure.

3. Results and Discussion

Fig. 4 shows the temperature distribution in the cross-sectional plane of the μ-TEG. In Type B structure, the temperature difference across the Si-NW, ΔT_{NW}, is slightly larger than that of Type A. The ΔT_{NW} of Type A and B structure is 0.767 K and 0.826 K, respectively. This is unexpected result because the thermal resistance of the heat guide increases by the shrinking. In this case, suppression of the heat injection effectively acts in maintaining the temperature difference.

In Type C structure, the ΔT_{NW} is slightly decreased from that of Type B, and it is almost the same value to that of Type A. By shrinking the device pitch, the injecting heat current density increases and thus the ΔT_{NW} is diminished.

However, from the view point of the areal output power density, Type C is the best. Fig. 5 shows the TE power of three structures. The TE power is proportional to the square of ΔT_{NW}. Thus, the TE powers of Type B and Type C are +4.1% and −1.2% compared with that of Type A, respectively. Fig. 6 shows the areal power density of three structures. The TE power density of the Type B and C is enhanced with +4.1% and +24% of the Type A, respectively. This result indicates that scaling the μ-TEG by shrinking both the hot side area and the device pitch is effective to enhance the TE performance.

4. Conclusions

We have pursued an optimum backend design of the cavity-free planar μ-TEG. We compared three different structures, and we found that the heat guide on the hot-side electrode is better to be narrowed to some extent to enhance the TE power output. Therefore, the device pitch can be further shrunk to improve the areal power density of the whole μ-TEG module. Present result shows that the output

power density is improved by at least 24%. By employing the optimum backend structure, the footprint of the μ-TEG is further suppressed, securing the scalability of the proposed planar μ-TEG architecture.

Acknowledgements

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References

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Table I thermal conductivity and interfacial thermal resistance set in the simulation

	κ [W/m·K]		$\theta_{interface}$ [K·m²/W]
Al	283	Al/AlN	15×10^{-9}
AlN	285	Al/SiO_2	7×10^{-9}
Si-Pad·Si-Sub	131	AlN/SiO_2	10×10^{-9}
Si-NW	1.4	Al/Si	20×10^{-9}
SiO_2	1.4	Si/SiO_2	2×10^{-9}

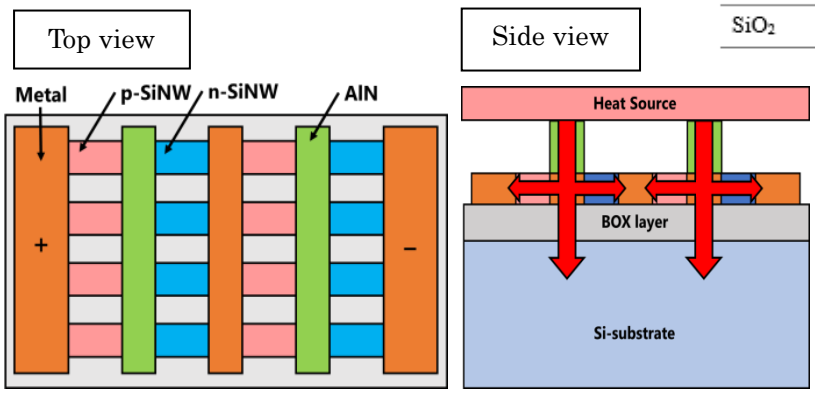

Fig 1 Schematic of the cavity-free μ-TEG.

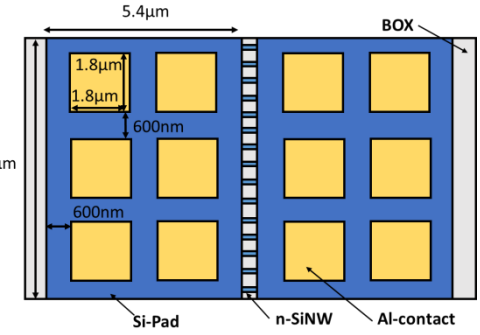

Fig2. Top view of SOI and Al-contact layer

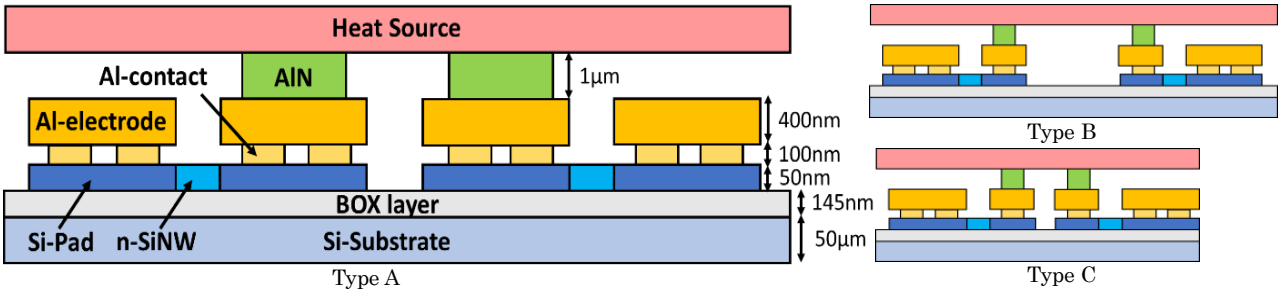

Fig 3 Cross-sectional view of 3 types μ-TEG structure.

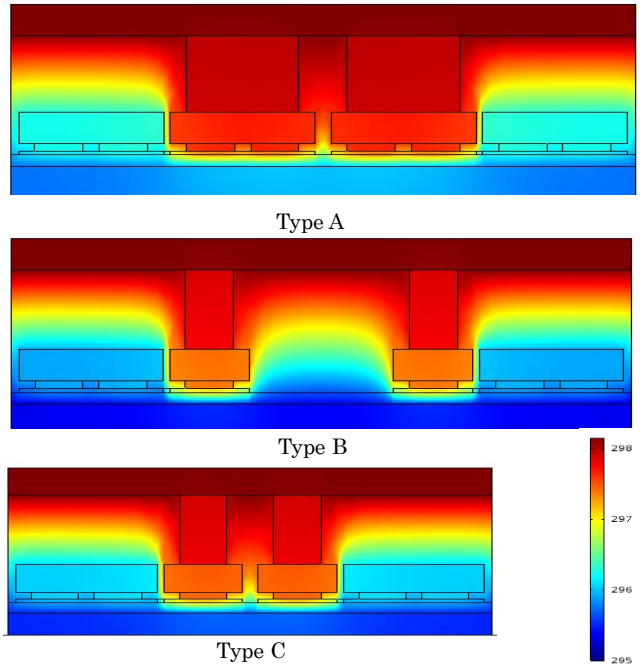

Fig.4 Cross-section temperature profile of μ-TEG.

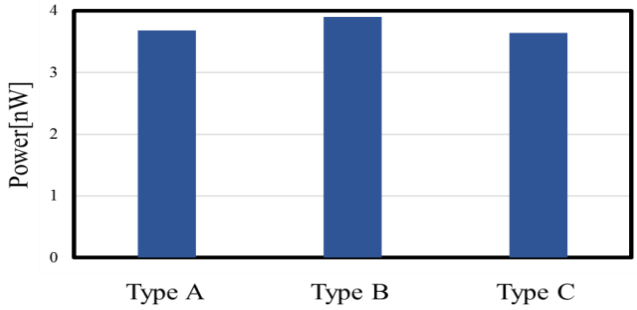

Fig.5 Comparison of TE power of three types of μ-TEG.

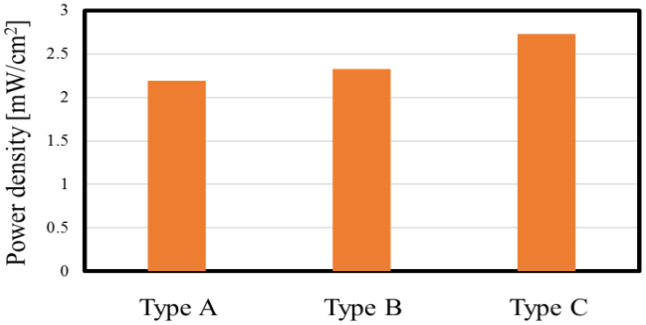

Fig.6 Comparison of areal power density.