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Continue the transistor scaling with 2D materials: Challenges and Perspective

Lain-Jong Li

Corporate Research, Taiwan Semiconductor Manufacturing Company (TSMC), 168 Park Ave.2, Hsinchu Science Park, Hsinchu 30075, Taiwan
e-mail: ljliv@tsmc.com

Internet of things and artificial intelligence demand further transistor performance improvements and device size scaling. In a conventional planar silicon field-effect transistor (FET), the gate controllability becomes weaker when its lateral dimension scales. Hence the transistor body thickness needs to be reduced to ensure efficient electrostatic control from the gate. When the silicon thickness reduces to a few nanometers, the fast mobility decay owing to the scatterings from imperfect silicon surfaces retards the further scaling.

New materials with perfect surfaces are therefore needed and 2D semiconducting materials such as MoS_2 and its analogues offer a chance to continue the scaling [1]. Many challenges are ahead for adopting these 2D semiconductors as FET channel materials, including (i) selection of 2D materials, (ii) reduction of contact resistance, (iii) growth of wafer-scale and single-crystalline 2D materials, and (iv) Integration of 2D materials to existing microelectronic fabrication processes. In this presentation, we will discuss on these challenges and possible approaches [2].

References:
[1] Ming-Yang Li, Sheng-Kai Su, H.-S. Philip Wong, Lain-Jong Li, Nature 567, 169-170 (2019).
[2] Sheng-Kai Su, Chih-Piao Chuu, Ming-Yang Li, H.-S. Philip Wong, Lain-Jong Li, Nature Nanotech. (submitted)