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High On/Off Ratio Tunnel Transistor Formed by CVD-grown Bilayer $WSe_2/MoSe_2$ van der Waals Heterostructures

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Abstract

Bilayer $WSe_2/MoSe_2$ van der Waals heterostructures have been directly grown on SiO_2/Si substrates by 2-step CVD method and band to band tunnel transistors with high on/off ratio larger than 10^6 have been demonstrated. Bilayer nature has been confirmed by Raman and TEM, while the device operation mechanisms have been explained based on gate-induced modulation of band alignment.

1. Introduction

Atomically thin transition metal dichalcogenides (TMDCs) have gained a lot of attention due to their attractive properties for future optoelectronic device applications. One of the interesting features of TMDCs is an availability of their vertical as well as lateral heterostructures with wide material variety, enabling us to explore band engineering to realize high performance novel devices such as band to band tunneling (BTBT) diodes/transistors, photosensors, and light emitting diodes etc. As for the vertical heterostructures, there is no lattice mismatch constrain thanks to van der Waals (vdW) stacking and BTBT devices with various combinations of 2D materials have been studied by using mechanical exfoliation/transfer technique [1-6]. On the other hand, for practical applications, CVD growth of TMDCs vdW heterostructures is inevitable and, in fact, direct CVD growth of bilayer TMDCs have been reported in a few pioneer works [7,8]. However, clear BTBT transistor operations have not been demonstrated yet in CVD-grown vdW heterostructures.

In this work, we have grown bilayer WSe_2/ $MoSe_2$ vdW heterostructures on SiO_2/Si substrates by 2-step solid source CVD and demonstrated the operation of tunnel transistor (TFET) with high on/off ratio larger than 10^6.

2. Experiment

All samples were grown by salt-assisted (KBr) solid source CVD method. In the first step, $MoSe_2$ was grown on the SiO_2 (285nm) /Si substrates by using MoO_2 and Se as precursors. Then, in the second step, WSe_2 was grown by using WO_3 and Se. The growth was conducted at 780 °C with a N_2/H_2 gas mixture using an electric furnace. After the growth, Ti/Au contacts were formed by lift-off processes both on top-layer WSe_2 and bottom-layer $MoSe_2$ (Fig. 1). Material characterizations were performed with Raman and TEM, while the electrical characterizations were carried out by using Si substrates as a back gate.

3. Results and discussion.

Figure 2 shows optical microscope image of as-grown sample. There can be seen three regions with different colors. The most inner triangular part is a bilayer region with top-layer WSe_2/bottom-layer $MoSe_2$, while the middle part corresponds to $MoSe_2$ monolayer without WSe_2. The most outer part is WSe_2 monolayer grown laterally from $MoSe_2$ edge, which is not further discussed in this paper. It should be noted here that previously reported CVD-grown $WSe_2/MoSe_2$ bilayer [5] showed different geometrical features from our samples, where 2nd layer growth started from the edge of the first layer, while in our case it certainly occurred from the center of the grain. Although the reason for this difference has not been verified, the obtained vdW heterostructures allowed us relatively easy device fabrication. It is also noted that the bottom- and top-layer grains are well aligned, reflecting energetical favored AB and AA' stacking. Figure 3 shows cross sectional TEM images of inner triangle region, showing reasonable thickness as bilayer $WSe_2/MoSe_2$ without distinct contaminations and defects at the vdW interface.

Figure 4 shows (a) Raman spectra from both $WSe_2/MoSe_2$ bilayer and $MoSe_2$ monolayer regions, (b) Raman mapping of the sample after electrodes formation. It is confirmed that two peaks corresponding to WSe_2 and $MoSe_2$ layers are observed in bilayer region, while only $MoSe_2$ peak is seen in monolayer region. Figure 5 shows I_d-V_d characteristics of the sample shown in Fig. 4(b). Here, source and drain (S/D) electrodes are formed on top-layer WSe_2 and bottom-layer $MoSe_2$, respectively. It is clearly seen that drain current (I_d) increases with increasing back gate voltage (V_{back}) and drain voltage (V_d). Since bottom $MoSe_2$ layer should be n-type doped with increasing V_{back} and n-type contacts could not be obtained in our CVD-grown monolayer WSe_2 (data not shown), this I_d is considered to originate in BTBT as shown in Fig. 6. On the other hand, suppressed I_d at $V_d < 0$ is attributable to Schottky barriers at S/D contacts, which should have minor effects under BTBT condition ($V_d > 0$). The photo-induced enhancement of OFF current and almost no change of ON current (Fig.7) is consistent with this model and indicates possible applications for photosensors. Figure 8 shows V_{back} dependence of I_d with varied V_d. Since ON current originates from BTBT as shown in Fig. 6, this large gate modulation of I_d with on/off ratio larger than 10^6 indicates successful operation of TFET. Figure 9 shows temperature dependence of (a) I_d-V_{back} characteristic and (b) subthreshold slope (SS) of the TFET. Although SS values are not appealing as TFET owing to very thick gate oxide and unoptimized gate oxide interface quality, insensitiveness of SS to temperature reflects the characteristic of BTBT current in TFET operation. The performance enhancement can be expected by optimizing device structure and device fabrication processes.

3. Conclusion

TFET with high on/off ratio of 10^6 have been demonstrated by using CVD-grown bilayer $WSe_2/MoSe_2$ vdW heterostructures.

CVD-grown bilayer TMDCs can provide not only fundamental research field for ideal 2D systems but also various types of applications utilizing BTBT phenomena.

Acknowledgements

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References

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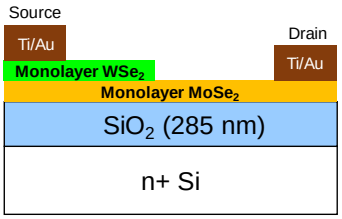

Fig. 1 Schematic picture of device structure with bilayer $WSe_2/MoSe_2$ vdW heterostructure.

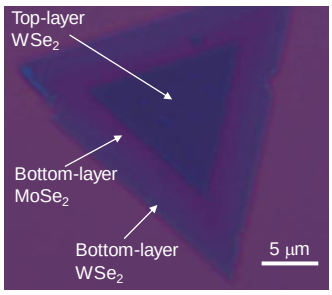

Fig. 2 Optical microscope image of bilayer $WSe_2/MoSe_2$ vdW heterostructure.

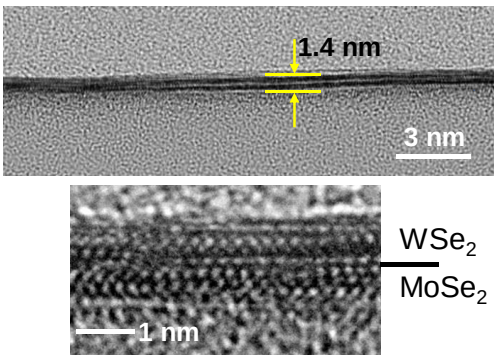

Fig. 3 Cross sectional TEM images of bilayer $WSe_2/MoSe_2$ vdW heterostructure.

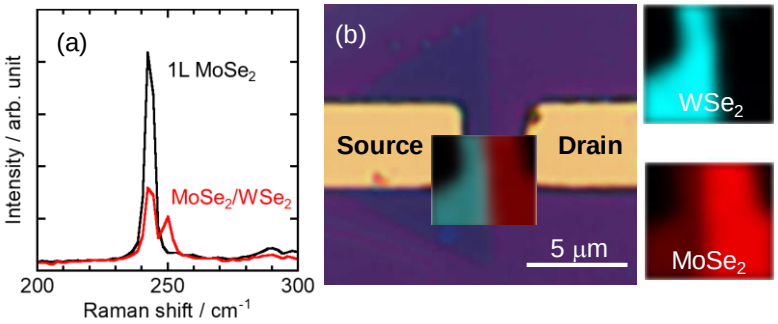

Fig. 4 (a) Raman spectra from bilayer $WSe_2/MoSe_2$ region and monolayer $MoSe_2$ region, (b) Raman mapping of fabricated device with S/D electrodes.

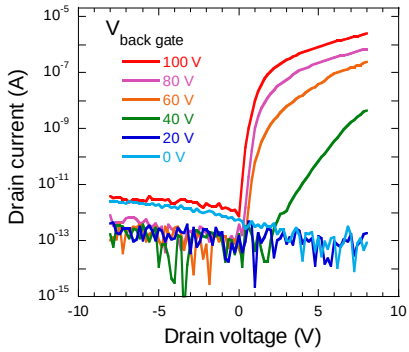

Fig. 5 V_{back} dependence of I_d-V_d characteristics.

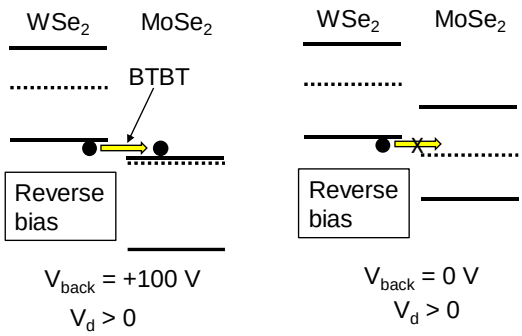

Fig. 6 Schematics of band aliment for gated $WSe_2/MoSe_2$ bilayer tunnel devices. In large positive V_{back} and positive V_d (reverse bias) condition, BTBT of electrons from valence band of WSe_2 to conduction band of $MoSe_2$ can take place.

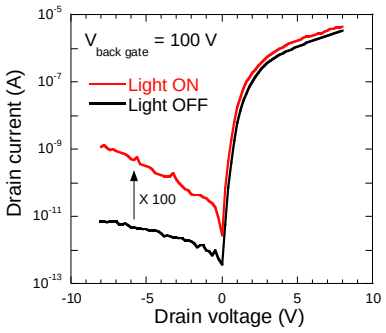

Fig. 7 Photo-induced change of I_d-V_d characteristic.

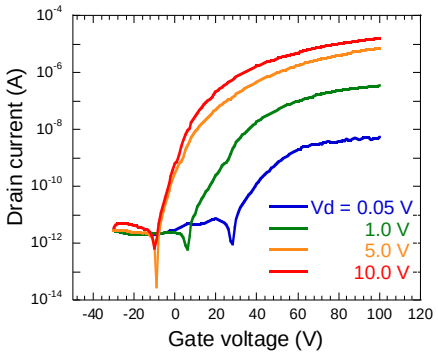

Fig. 8 I_d-V_g characteristics of $WSe_2/MoSe_2$ TFET with varied V_d.

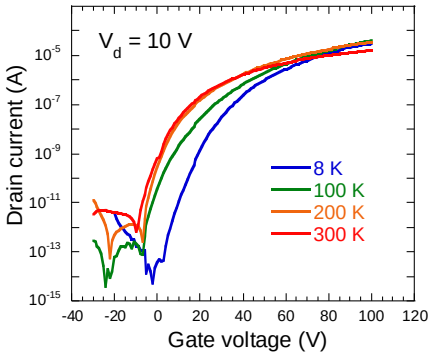

Fig. 9 Temperature dependence of I_d-V_g characteristics of $WSe_2/MoSe_2$ TFET.

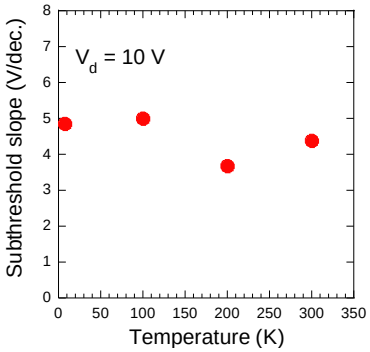

Fig. 10 Temperature dependence of SS of $WSe_2/MoSe_2$ TFET.