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Scalable Nanomanufacturing Processes for High Performance Transistor Inks

Maritza Mujica*, Amar T. Mohabir*, Gozde Tutuncuoglu, Victor Breedveld, Sven H. Behrens, Eric M. Vogel, Michael A. Filler

Georgia Inst. of Tech.
Georgia, GA 30332, USA
Phone: +1-404-894-0430 E-mail: mfiller@gatech.edu

Abstract

We present a suite of new nanomanufacturing processes to fabricate, in an entirely bottom-up fashion, high performance modular semiconductor devices. The Geode and SCALES processes enable compositionally-encoded semiconductor nanowire synthesis and nanoscale patterning thereof at rates orders-of-magnitude beyond the state-of the-art. Our approach promises dispersions of "plug-and-play" building blocks suitable for all manner of massively-scalable electronic and photonic systems.

1. Introduction

Despite the speed (i.e., > GHz), energy efficiency (i.e., < 1 V), and relatively low cost of Si wafer-based integrated circuits, many situations exist where their cost, quantity, form factor, and/or functionality are inadequate. For example, the high throughput manufacturing of large-area integrated circuits (e.g., >> 1 m^2) would dramatically expand the number of use-cases for electronic systems. A variety of new materials (e.g., organics, oxides, nanocrystals, carbon nanotubes, and 2-D materials) and patterning techniques (e.g., nanoimprint, inkjet) have been explored for this purpose. Unfortunately, state-of-the-art devices, due to low carrier mobilities, large contact resistance, and the challenge of creating nanoscale channels at high manufacturing rates, still exhibit switching speeds and supply voltages substantially inferior to Si. This poor performance renders these devices inadequate for many key circuit functions, including low-power/high-speed computation and long-distance wireless communication. While hybrid approaches have emerged in recent years, wafer-based fabrication as well as pick-and-place processes fundamentally limit the possible manufacturing scales and cost floor.

The vapor-liquid-solid (VLS) mechanism, which allows for the bottom-up growth and nanoscale compositional encoding of single-crystalline semiconductor materials (i.e., groups IV, III-V, and oxides), is a promising route to the high performance materials and devices need for large-area electronics. However, it remains constrained by (i) the limited production rates possible on macroscopic, flat surfaces and (ii) the need for top-down lithography to define key device features (e.g., contacts, gate stacks) and spatially control the deposition of thin films.

2. Objectives

The present work describes two new nanomanufacturing processes – Geode [1] and SCALES [2] – to enable the fully bottom-up manufacturing of high performance electronic and photonic devices.

The Geode process [1] utilizes an unconventional substrate to significantly increase nanowire production rates: the interior surface of hollow silica microcapsules lined with the metal nanoparticles that seed nanowire growth. Hollow microcapsules offer several benefits: (1) large substrate area that scales with the sample (i.e., microscapsule powder) volume, (2) prevention of nanowire agglomeration, (3) physical protection of the nanowires and seed particles during processing, and (4) decoupling of nanowire dimensions and reactor flow behavior (i.e., eliminates the need to successfully entrain nanowires in a low density gas).

The SCALES (Selective CoAxial Lithography via Etching of Surfaces) process [2] leverages chemical differences between encoded segments to yield surface masks with nanoscale precision. Such masks can subsequently direct the deposition of the thin films (e.g., oxides, metals) needed to complete the construction of fully-functional devices.

3. Methods

The Geode Process. Hollow microcapsules with their interior surface decorated by Au nanoparticles, for use in the Geode process, are produced with a scalable double emulsion/solvent extraction technique. A schematic of the microcapsule assembly is shown in Figure 1.

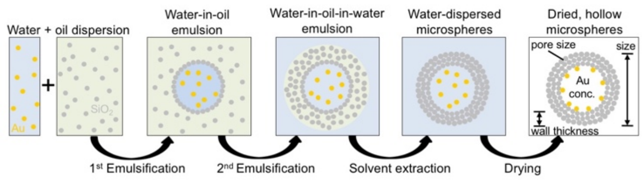

Fig. 1 Steps in the production of hollow silica microcapsules as nanowire growth substrates.

In the first step, an aqueous dispersion of the gold nanoparticles is emulsified in an organic solvent ("oil") containing hydrophobized silica particles. The resulting water-in-oil emulsion is in turn emulsified in an outer aqueous phase, yielding water-in-oil-in-water double emulsion droplets with an aqueous core surrounded by a liquid shell of oil-based silica dispersion. If the solvent in the oil phase is chosen to have some residual water-miscibility and higher vapor pressure than water, it can easily be extracted by evaporation and/or dilution with the outer aqueous phase. This step then leaves behind the originally oil-dispersed hydrophobic silica particles in the form of solid spherical shells (i.e., hollow microcapsules), templated by the inner aqueous droplets. Upon drying of the hollow microcapsules, the gold nanoparticles originally dispersed inside deposit on the inner microcapsule walls, where they can then catalyze nanowire growth.

The SCALES process. SCALES occurs in three steps: (1) Synthesis of a nanowire with a suitable compositional heterogeneity, (2) surface-initiated polymerization of a suitable masking material, and (3) selective removal of the mask, as shown in Figure 2, only from nanowire segments whose underlying surface is susceptible to an etchant. Poly(methyl methacrylate) (PMMA) is used as the mask in the present work and is grown via atom transfer radical polymerization (ATRP). The choice of etchant depends on the compositional encoding of the nanowire. For model Si/Ge systems, we leverage differences in the chemistry of SiO_x and GeO_x surfaces to selectively etch Ge but not Si in H_2O_2 solution.

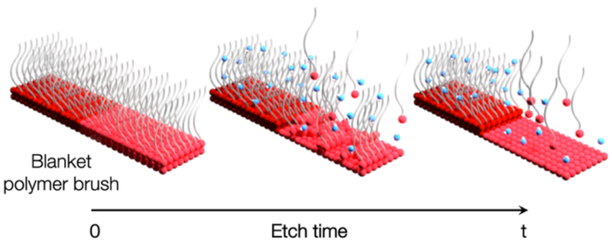

Fig. 2 Illustration of polymer removal step of the SCALES process. An etchant diffuses through the grafted polymer layer and selectively removes surface atoms from one region but not another.

4. Results

Figure 3 shows the scalable emulsion templating of hollow microcapsules that are decorated on their interior surface with Au nanoparticles to catalyze nanowire growth. The demonstrated growth of dense, good morphology nanowires on the interior of hollow microscapsules shows that gases can traverse the porous wall at sufficiently high transfer rates to enable growth. Au nanoparticles are observed at the nanowire tips, indicating growth via the VLS mechanism. Successful microcapsule drying is strongly influenced by silica particle type as well as the use of a particle crosslinking agent.

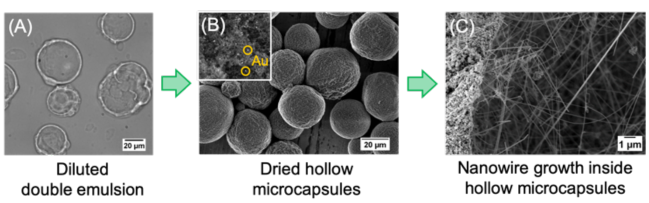

Fig. 3 Demonstration of hollow microcapsule synthesis and nanowire growth via the VLS mechanism.

Figure 4 shows transient XPS and ellipsometric measurements confirming selective polymer removal on Si and Ge wafers. The C(1s) photoelectron peak intensity decreases on Ge surfaces, where PMMA is removed, but not on Si. Ellipsometry corroborates the XPS data.

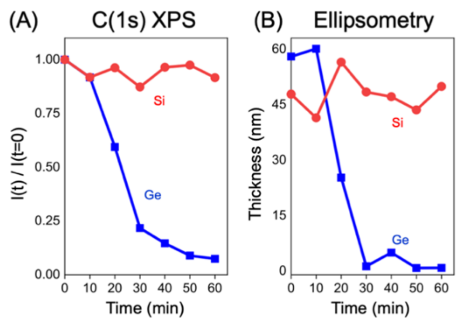

Fig. 4 Normalized intensity of C(1s) photoelectron peak for PMMA-coated Si and Ge wafers as a function of exposure time to H_2O_2. The PMMA is selectively removed from Ge but remains on Si. (B) Complimentary characterization with ellipsometry reveals the same behavior.

5. Conclusions

The Geode and SCALES processes constitute a powerful new platform with which to fabricate and deploy high performance semiconductor devices and systems at very large scales.

Acknowledgements

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References

[1] M. Mujica, G. Tutuncuoglu, A. T. Mohabir, V. Breedveld, S. H. Behrens, and M. A. Filler, submitted (2019).
[2] A. T. Mohabir, G. Tutuncuoglu, T. Weiss, E. M. Vogel, M. A. Filler, submitted (2019).

Appendix

Secretariat of SSDM2019
c/o KNT-CT Global Travel CO., LTD. Global MICE Department
E-mail: secretariat@ssdm.jp
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