Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp183-184

Artificial Synapse based on MoS_2 Memtransistor for Neuromorphic Computing

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***Abstract*—We report the demonstration of multi-terminal memtransistors using wafer-scale polycrystalline monolayer MoS_2 synthesized *via* chemical vapor deposition (CVD). The memtransistors exhibit prominent gate-tunable bidirectional resistive switching behavior, with the highest switching ratio exceeding 10^4. The non-volatile memory functions further augment the operation of artificial synapses as exemplified by the long-term plasticity, spike-amplitude and spike-timing-dependent plasticity under various pulse conditions. More notably, the memtransistors allow both gate and drain terminals to serve as the stimulus input in a single synaptic cell, thus offering extra degree of freedom for realizing complex neuromorphic computing.**

1. Introduction

As a fundamental component in neuromorphic computing, analog synapses have been extensively investigated in many non-volatile memory devices [1]. Recently, gate-tunable memristors (or memtransistors) have been proposed for potential exploitation in neuromorphic systems [2-3]. However, in previous works, the operating voltages for resistive switching (RS) are high (30 V) and the switching ratio is relatively low (~500) as compared with memristor of other types. Here, we report MoS_2-based memtransistors on as-used sapphire substrate. Exhibiting widely-tunable analog RS with switching ratios higher than 10^4, the devices possess great potential for neuromorphic application, by emulating synaptic long-term plasticity, spike-amplitude and spike-timing-dependent plasticity. Particularly, what distinguishes our artificial synapses from previous ones is the ability to enable either gate or drain terminal to serve as presynaptic input [4-5], thus permitting additional degree of freedom in the design of neuromorphic circuits.

2. Device Fabrication

Continuous polycrystalline film of monolayer MoS_2 was grown *via* CVD on sapphire substrate (Fig. 1) [6]. Atomic force microscopy (AFM) reveals MoS_2 with grain sizes of 1-4 μm (Fig. 2). Active areas of devices were defined by CHF_3-based reactive-ion etching. Source, drain and gate electrodes (Ti/Au) were formed by electron beam lithography and photolithography, thermal evaporation, and lift-off processes. A 20 nm thick HfO_2 was grown by atomic layer deposition to serve as the gate dielectric. Devices with various channel lengths were fabricated, with the smallest being 200 nm (Fig. 3). Electrical measurements were carried out with a semiconductor parameter analyzer (Keithley 4200) equipped with pulse measurement units.

3. Results and Discussion

We first characterized the device by sweeping V_{ds} in a closed loop at V_{gs} = 0 V. Fig. 4 shows the result of 160 consecutive sweeps on a representative device with 400 nm channel length. Apparently, the device displays significant bipolar analog RS behavior. A positive scan (0 to -10 V) towards higher V_{ds} biases gradually switches it from high resistance state (HRS) to low resistance state (LRS) and retains its LRS for V_{ds} sweep from 10 back to 0 V. A reset to HRS can be achieved by sweeping a negative V_{ds} (0 to -10 V) and the HRS is maintained for V_{ds} from -10 to 0 V. Inspiringly, a switching ratio (R_{HRS}/R_{LRS}) of higher than 10^4 is obtained which outperforms previously reported devices of similar configuration, rendering the device promising for large dynamic range neuromorphic application.

The dependence of RRAM characteristics on V_{ds} sweep range and gate bias is further investigated. In Fig. 5, the HRS and LRS resistances of the device are shown to be largely affected by the V_{ds} sweep range, which could be attributed to a more pronounced defect migration and charge trapping/detrapping process [7]. Consequently, the difference between HRS and LRS shrinks with reduced V_{ds} range, with the switching ratio changing from >10^4 for ±12 V V_{ds}, to 34 for ±6 V V_{ds}. In Fig. 6, the advantage of integrating RS within a transistor structure is demonstrated. By varying V_{gs} from -6 V to 4 V, both the HRS and LRS manifest a decent gate tunability, resulting in a tunable switching ratio from 500 to 10 for V_{gs} = -6 V and V_{gs} = 4 V, respectively. A more remarkable gate dependence can be fully expected for a wider range of V_{ds}.

Gradual RS holds great promise for mimicking the dynamic activities of biological synapses (Fig. 7). In Fig. 8, by introducing the electrical stimulus (voltage pulses) to the drain, the ability of the device to emulate typical synaptic behaviors is demonstrated. Specifically, a positive and negative V_{ds} pulse train induces positive and negative changes in the post-synaptic current (PSC, I_{ds}), corresponding to long-term potentiation (LTP) and long-term depression (LTD), respectively. Fig. 8a presents the evolution of PSC under consecutive pulse sequences with varying pulse amplitude. The change in PSC after 50 pulses of each sequence exhibits an enhancement with increasing V_{ds} pulse amplitude (Fig. 8b inset), manifesting spike-amplitude-dependent plasticity (SADP). STDP is another important functionality for the learning and memory purpose of a synapse. In Fig. 8c, positive (negative) changes in the synaptic weight are induced by paired positive (negative) V_{ds} pulses, with longer time interval leading to weaker potentiation (depression), indicating good emulation of STDP.

Furthermore, the gate terminal of the memtransistor can be used as another presynaptic input. When the gate bias is swept in a closed loop, huge hysteresis is observed (Fig. 9a), which is much larger than that reported in floating-gate transistors-based synapses. The hysteresis behavior is primarily attributed to the defects in the polycrystalline MoS_2 such as grain boundaries and sulfur vacancies. On the basis of a large gate hysteresis, by applying different negative/positive pulse sequences to the gate, synaptic activities such as long-term-plasticity (Fig. 9b-c) and SADP (Fig. 9d) are clearly demonstrated.

4. Conclusion

In summary, monolayer MoS_2 memtransistors with prominent and widely-tunable RS properties are demonstrated. The devices hold promise for synaptic emulators and neuromorphic computing with excellent flexibility in deploying either gate or drain as the presynaptic input, an attribute not possessed by conventional two-terminal devices. Furthermore, the wafer-scale MoS_2 growth and CMOS-compatible device fabrication process in this work imply straightforward scalability for realizing high performance large-scale neuromorphic circuits.

Acknowledgment

This research is supported by A*STAR Science and Engineering Research Council (Grant Nos. 152-70-00013, 152-70-00012), and by the National Research Foundation, Prime Minister's Office, Singapore.

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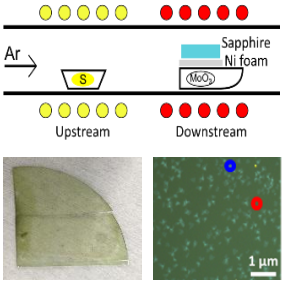

Fig. 1. (Top) Illustration of MoS_2 growth using sulfur and MoO_3. (Below) Photographs of CVD-grown polycrystalline monolayer MoS_2 on transparent sapphire substrate.

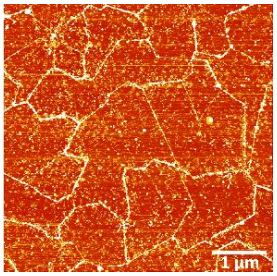

Fig. 2. Scanned atomic force microscopy (AFM) phase channel image in tapping-mode. Grain boundaries are noticed in MoS_2 with grain sizes of 1~4 μm.

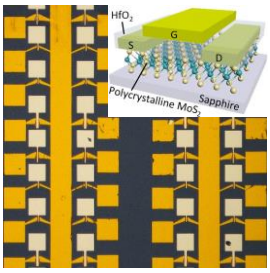

Fig. 3. Fabricated MoS_2 devices on sapphire. Inset is schematic of the MoS_2 memtransistor. Ti/Au was used for electrodes, and 20 nm HfO_2 for gate dielectric.

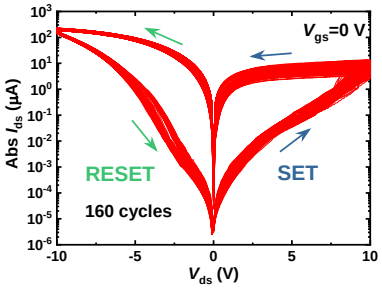

Fig. 4. Looped I_{ds}-V_{ds} of the MoS_2 memristor for 160 sweep cycles at V_{gs}=0 V, showing distinct resistive switching with >10^4 switching ratios. Currents at V_{ds}=0.1 V are used for calculation.

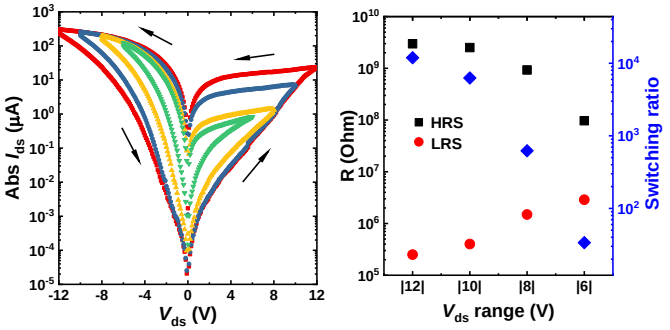

Fig. 5. (Left) Dependence of memristive behavior on V_{ds} sweep range. (Right) Extracted HRS and LRS resistance at V_{ds}=0.1 V, and switching ratio as a function of V_{ds} range. An increase of switching ratio with V_{ds} sweep range is observed.

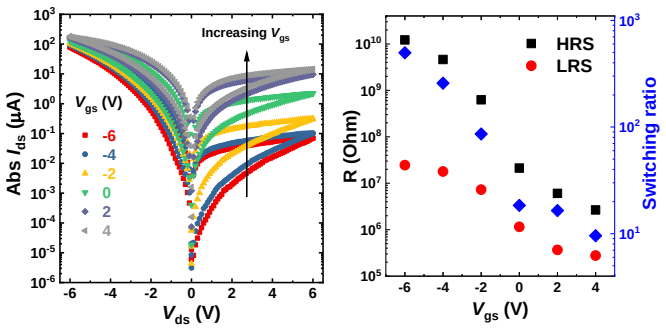

Fig. 6. (Left) Gate-tunability of memristive behavior demonstrated in the MoS_2 memtransistor. (Right) Extracted HRS and LRS resistance at V_{ds}=0.1 V, and switching ratio as a function of V_{gs}.

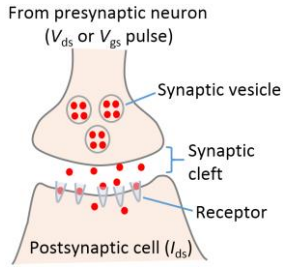

Fig. 7. Schematic of a synapse where presynaptic irritation can be introduced to both V_{ds} and V_{gs}, while PSC is represented by I_{ds}.

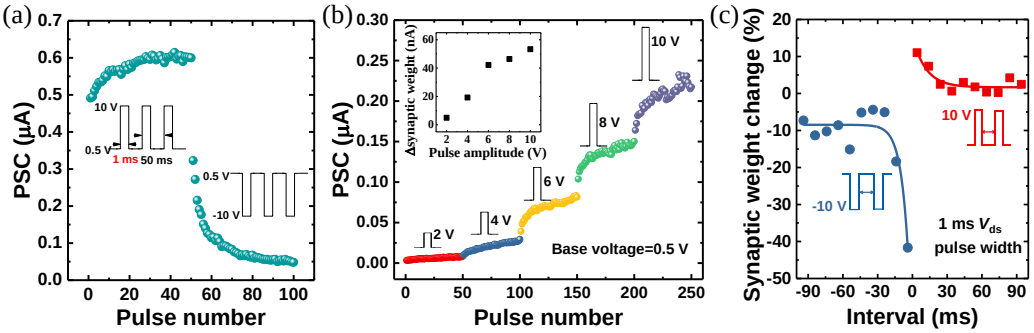

Fig. 8. (a) PSC *versus* number of pulse on V_{ds}, showing long-term potentiation (LTP) and depression (LTD). (b) PSC *versus* pulse number with varying V_{ds} pulse amplitude. Inset shows enhanced potentiation with increasing pulse amplitude. (c) Synaptic weight change dependence on the time interval between paired V_{ds} pulses. The solid lines are exponential fits with time constants of 11.6 ms and 6.5 ms for positive and negative pulses, respectively.

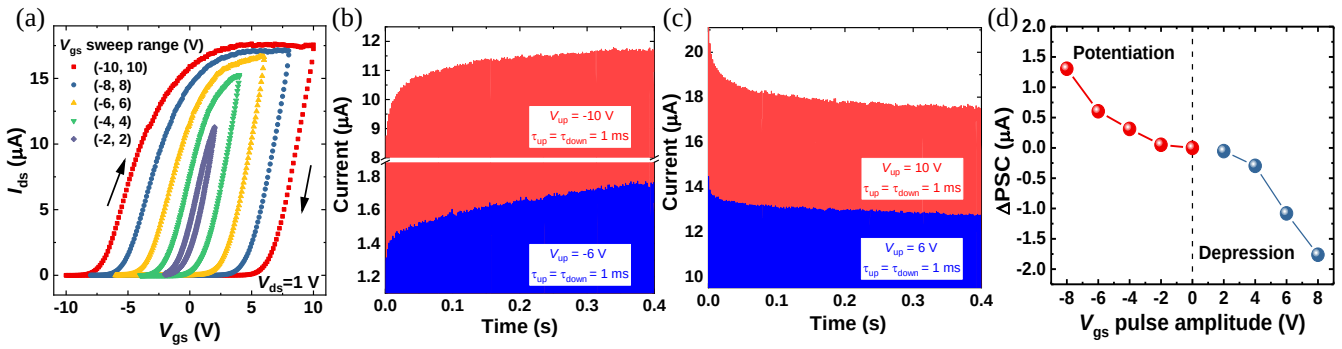

Fig. 9. (a) Transfer characteristics of a MoS_2 memtransistor with channel length L=400 nm, showing hysteresis that increases with V_{gs} sweep range. (b) Dynamic response of the synapse to a sequence of 200 V_{gs} pulses with −10 V (red) and −6 V (blue) pulse amplitude, showing progressive synapse potentiation. (c) Dynamic response of the synapse to a sequence of 200 V_{gs} pulses with 10 V (red) and 6 V (blue) pulse amplitude, showing progressive synapse depression. Pulse width = 1 ms and pulse period = 2 ms. A higher pulse amplitude results in a more-efficient potentiation (for negative V_{gs} pulse) or depression (for positive V_{gs} pulse) process. (d) Change in PSC, showing an increasing impact of increasing V_{gs} pulse amplitude. V_{gs} pulses are applied with 0 V base. Current is read at V_{ds}=0.5 V.