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High Performance Three-Terminal Synaptic Transistor based on Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$/Tungsten Disulfide for Neuromorphic Computing

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ABSTRACT

This work demonstrates for the first time a high performance synaptic transistor based on tungsten disulfide (WS_2) and ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO). The as-fabricated transistor achieves a large hysteresis due to the polarization hysteresis of HZO. A high current on/off ratio of ~10^5 at V_G = 0 V between two voltage sweep directions is obtained. Moreover, the hysteresis is further utilized to mimic the neurotransmitter release dynamics in biological synapse. A large current ratio of over 10^3 between the excitatory post-synaptic current (PSC) and inhibitory PSC is well matched to the potentiation and depression behavior of typical synapses, showing potential for next generation neuromorphic computing applications.

Keywords: WS_2, ferroelectric HZO, synaptic transistor, PSC, neuromorphic computing

INTRODUCTION

Neuromorphic computing system has been considered as a promising candidate beyond conventional von-Neumann computer architecture in performing cognitive tasks [1, 2]. As a basic component in neuro-inspired architecture, analog synapses have been extensively investigated in many devices, such as three terminal synaptic transistors [3, 4], where the signal transmission is *via* the channel while the synaptic weights are modulated independently *via* gate terminal. This configuration allows the signal transmission and learning function to be performed simultaneously, providing more flexible operation for signal processing and learning in synaptic circuits. At the same time, two-dimensional (2D) materials have attracted growing interests owing to their ultra-thin geometry and unique electronic properties, which allows for aggressive scaling and excellent electrostatic control. However, there is still a lack of synaptic transistors using 2D materials as the channel materials.

Here, we propose an integration flow to realize 2D WS_2 and ferroelectric HZO based synaptic transistor. A large hysteresis is achieved in the transistor, which is induced by the polarization hysteresis of the HZO ferroelectric gate stack. This hysteresis engineering is further deployed to emulate the synaptic plasticity of biological synapses. The essential synaptic behaviours, such as excitatory PSC, potentiation and depression of the synaptic weight are demonstrated in the three-terminal synaptic transistor, showing great potential towards the applications of neuromorphic computing system and artificial intelligence.

DEVICE FABRICATION

Fig. 1 shows the key process for realizing the HZO/WS_2 based synaptic transistor. Heavily doped Si is employed as the conducting back gate electrode. 6 nm HZO and 2 nm Al_2O_3 are deposited on the substrate by ALD as the ferroelectric gate stack and capping layer, respectively. Then, rapid thermal annealing (RTA) process at 500 ˚C is carried out to crystallize the HZO and enhance its ferroelectricity. Thereafter, a 8 nm WS_2 flake is mechanically exfoliated onto the wafer, followed with the source/ drain metal electrode patterning and deposition by e-beam lithography and e-beam evaporator, respectively. **Fig. 2** shows the three dimensional schematic structure of the device and the SEM image is shown in **Fig. 3**. The channel length and width of the synaptic transistor are 500 nm and 8 μm, respectively.

RESULTS AND DISCUSSION

A. Characteristics of WS_2 flake and ferroelectricity of HZO gate stack

The Raman spectrum of the WS_2 flake shows two dominant phonon peaks at 351.3 cm^{-1} and 421.5 cm^{-1}, which corresponds to the in-plane phonon mode and out-plane phonon mode as shown in **Fig. 4**, respectively, which is in agreement with previous work [5]. *P-V* measurements on Au/Ti/Al_2O_3/HZO/P^{++} Si capacitor with different RTA temperature are conducted to examine the ferroelectricity of HZO. Notably, HZO shows stronger ferroelectricity after RTA at 500 ˚C, while HZO without anneal shows nearly no polarization hysteresis as shown in **Fig. 5**. This phenomenon is further confirmed by the TEM analysis as shown in **Fig. 6**. Poly crystallization of HZO is realized after the annealing process, which enhances the ferroelectricity of HZO gate stack. **Fig. 7** shows the EDX analysis of the device, confirming the composition of WS_2 and $Hf_{0.5}Zr_{0.5}O_2$ layers.

B. DC measurement results of the synaptic transistor

Fig. 8 shows the transfer characteristics of the synaptic transistor. Large hysteresis is observed between forward and backward scans, resulting from the polarization hysteresis of the HZO ferroelectric layer. The HZO ferroelectric gate stack efficiently modulate the threshold voltage of the synaptic transistor. Typically, the forward sweep causes a positive threshold voltage (V_{TH}) whereas the backward sweep results in a more negative V_{TH}, which is in contrast with the phenomenon of V_{TH} shift caused by charge trapping as illustrated in **Fig. 9** [6]. This behavior leads to two current states of the transistor at V_G = 0 V, which can be applied to synaptic devices. The current on/off ratio at V_G = 0 V is extracted in **Fig. 10**. Inspiringly, an on/off ratio of ~10^5 is achieved when the V_G scanning range is up to 3.5 V, outperforming other reported work with similar configuration. Simultaneously, the difference of V_{TH} is extracted to be linearly increased between two sweep directions with the V_G scan range as shown in **Fig. 11**, confirming that such hysteresis behavior is due to the polarization hysteresis of the HZO ferroelectric layer.

C. Pulse measurement results of the synaptic transistor

Pulse measurements are performed on the as-fabricated synaptic transistor. Consecutive rectangular positive and negative pulse sequences of the same absolute pulse amplitude are applied to induce positive and negative changes in the PSC (I_{ds} at V_G = 0 V), as shown in **Fig. 12**. The PSC exponentially increases with positive pulse cycle numbers to reach long-term potentiation effect; whereas a negative pulse decreases the PSC to achieve long-term depression effect. This behavior holds great promise for mimicking the dynamic activities of typical biological synapses. The excitatory PSC increases with the pre-synaptic spike weight (the amplitude of positive pulse) as shown in **Fig. 13**, implying the ability of synaptic transistor in responding to distinct stimuli. Simultaneously, the large synaptic weight change ratio between excitatory and inhibitory PSC of over 10^3 is achieved when the absolute pulse amplitude is above 3 V as shown in **Fig. 14**. **Fig. 15(a)** shows the dynamic response of the device. The peak excitatory PSC (read at V_G = 3.5 V) increases with stimulation time, while PSC drops to a relatively stable state when the device is unbiased after 15 cycles as shown in **Fig. 15(b)**. The relaxation time constant is extracted to be ~0.38 ms by exponential fitting as shown in **Fig. 16**. **Fig. 17** shows the relationship between PSC and pulse interval time. Typically, larger interval time between two pulses results in a lower PSC. To better evaluate the performance of our HZO/WS_2 based synaptic transistor, a comparison among the reported synaptic transistors is carried out as shown in **Fig. 18**. Our device achieves a relatively high current on/off ratio at V_G = 0 V and a relatively high PSC change, outperforming other reported works [3-4, 7-11].

CONCLUSION

Three-terminal synaptic transistor based on 2D WS_2 channel material and ferroelectric HZO gate stack is successfully demonstrated. A record combination of PSC and on/off ratio up to five orders-of-magnitude is achieved. Additionally, the large hysteresis enables the devices to mimic the synaptic plasticity of biological synapses, rendering it promising for enabling neuromorphic learning application.

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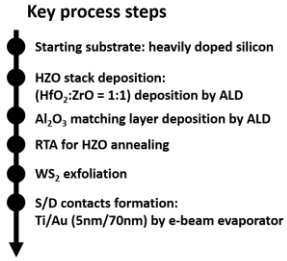

Fig. 1. Process flow for realizing HZO & WS_2 based synaptic device.

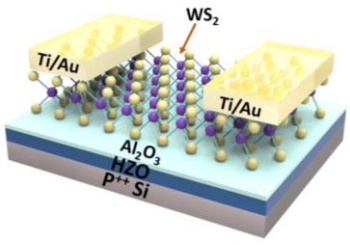

Fig. 2. Three-dimensional structure of HZO/WS_2 based synaptic device.

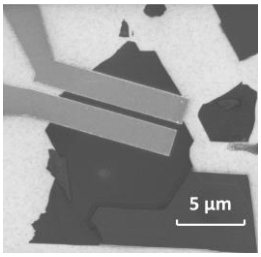

Fig. 3. SEM image of HZO/WS_2 synaptic transistor. Channel length and width are 500 nm and 8 µm, respectively.

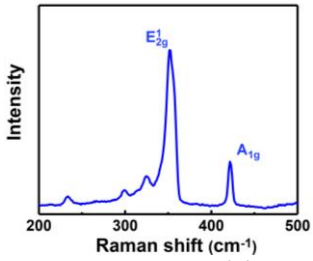

Fig. 4. Raman spectrum of few-layer WS_2 flake, showing 2 dominant phonon peaks at 351.3 cm^{-1} and 421.5 cm^{-1}.

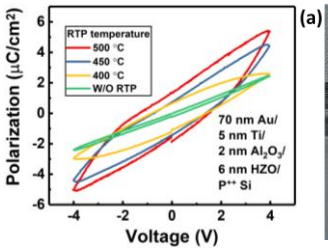

Fig. 5. *P-V* measurement on Au/Ti/Al_2O_3/HZO/P^{++} Si capacitor. HZO ferroelectricity is prominently enhanced after RTP anneal.

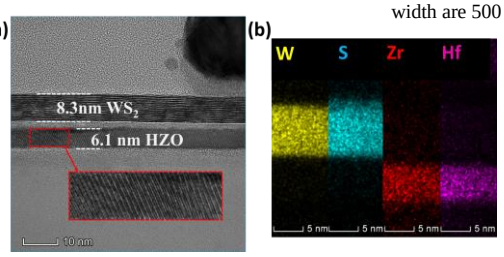

Fig. 6. TEM image of HZO/WS_2 based synaptic transistor. (a) The thickness of WS_2 is ~8 nm. The poly crystallization of ~6 nm HZO after the RTP annealing is seen. (b) EDX mapping shows the relative intensity of the core elements.

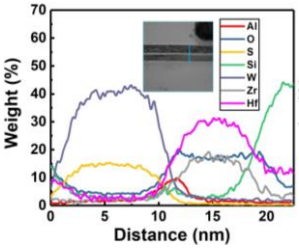

Fig. 7. The weight ratio of elements in HZO/WS_2 based synaptic transistor.

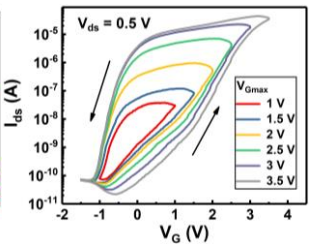

Fig. 8. Transfer characteristics showing enhanced hysteresis when the V_G scan range is increased.

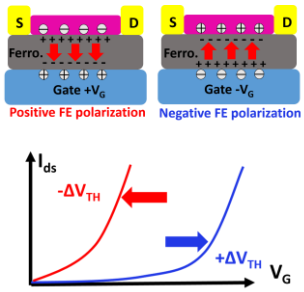

Fig. 9. Schematic illustration of threshold voltage shift caused by the ferroelectric polarization.

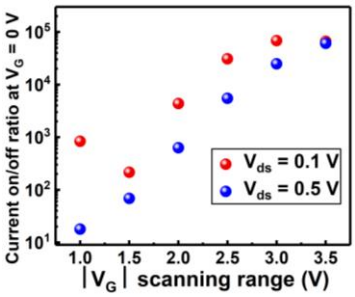

Fig. 10. Extraction of the current change at V_G = 0 between backward and forward scan. The current difference increases with V_G scanning range.

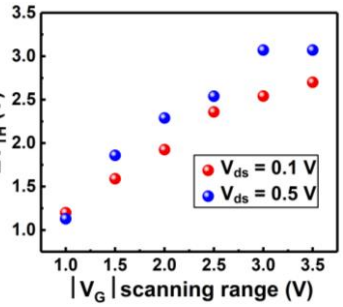

Fig. 11. Extraction of ΔV_{TH} versus V_{Gmax} range for V_{ds} = 0.1 V and V_{ds} = 0.5 V, the ΔV_{TH} linearly increases with V_G scanning range.

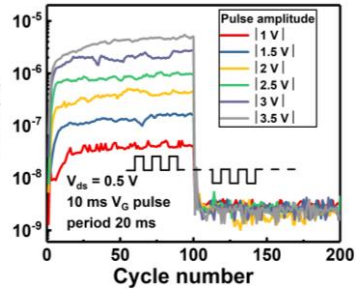

Fig. 12. PSC versus pulse cycle numbers. A series of positive rectangular V_G pulse followed with negative V_G pulses of 10 ms width are applied to induce PSC changes.

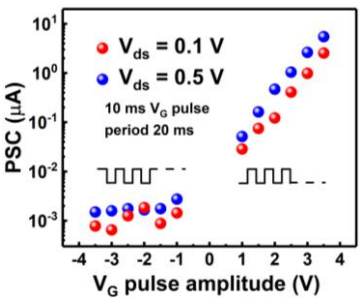

Fig. 13. The PSC increases dramatically with the positive V_G amplitude, and decreases with negative V_G amplitude after 100 pulse cycles.

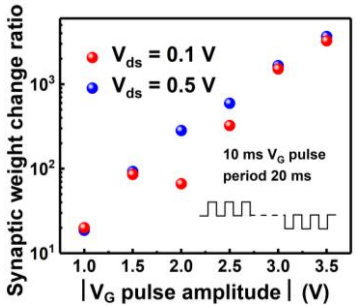

Fig. 14. Extraction of PSC weight change ratio versus |V_G pulse amplitude|, showing increasing ratio between two states with increasing pulse amplitude.

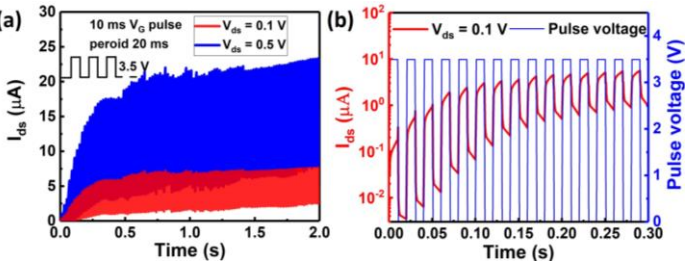

Fig. 15. Dynamic response of the HZO/WS_2 based synapses. (a) The peak excitatory PSC increases with the stimulation time. (b) Zoomed in plot of (a), showing that the PSC remains relatively stable state after 15 pulse cycles.

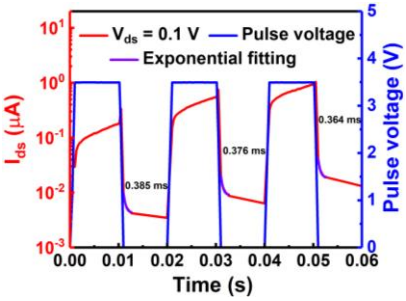

Fig. 16. Relaxation characteristic of the HZO/WS_2 based synapses, showing a relaxation time constant of ~ 0.38 ms.

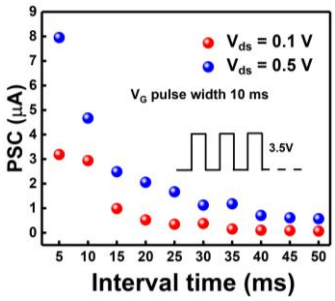

Fig. 17. PSC versus pulse interval time, showing larger PSC when the interval between two pulses is reduced.

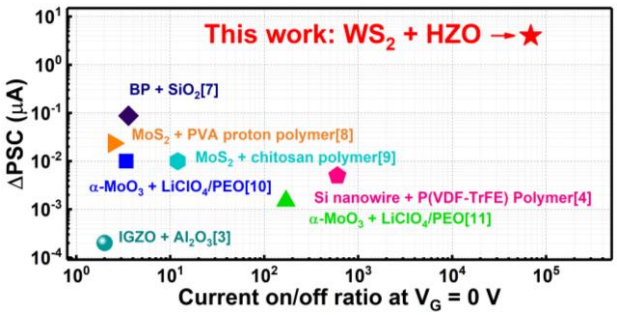

Fig. 18. Benchmarking of recently reported synaptic transistors. Our HZO/WS_2 synaptic transistor achieves a relatively high current on/off ratio at V_G = 0 V and high PSC change compared with other reported works.

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