Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp193-194

Growth and electrical properties of in-situ doped GeSn nanowires for low power tunnel Field Effect Transistor.

T. Haffner[1], F. Bassani[1], P. Gentile[2], N. Pauc[2], E. Martinez[3], T. Baron[1], E. Robin[4], S. David[1], B. Salem[1]

[1]Univ. Grenoble Alpes, CNRS, LTM, 38000 Grenoble, France

[2]Univ. Grenoble Alpes, CEA, INAC-Pheliqs, 38000 Grenoble, France

[3]Univ. Grenoble Alpes, CEA, LETI-DTSI, 38000 Grenoble, France

[4]Univ. Grenoble Alpes, CEA, INAC-MEM, 38000 Grenoble, France

Abstract

As Tunnel FET shows promising results for future low power device, they still suffer from low ON current. We will present a novel approach to design enhanced ON current TFET based on GeSn group IV low bandgap alloy grown by chemical vapor deposition (CVD) using the vapour-liquid-solid (VLS) mechanism. Single GeSn nanowire (NW), in-situ doping and heterostructured p-i-n NWs will be investigated.

1. Introduction

Tunnel Field Effect Transistors (TFET) have attracted tremendous interest for future ultra-low power device due to their potential sub 60 mV/dec subthreshold swing at room temperature. Several work demonstrated sub-60mV/dec SS [1] or high-ON current [2] on silicon. However, achieving a simultaneous low SS and high-ON drive current is still challenging as silicon have a relatively large and indirect bandgap. Hence, research were lead on direct, low bandgap material such III-V alloys [3], demonstrating high drive current but still high SS, mainly attributed to the poor high-*k*/channel interface. Recently, group IV GeSn alloy was demonstrated as a potential candidate for further pTFETs integration [4]. Indeed, GeSn exhibit a low bandgap with indirect to direct nature transition for Sn concentration above 8% [5, 6] and show promising results in terms of high-*k*/GeSn interface [7]. However, due to the high lattice mismatch between Ge and Sn (≈14%) and the low solubility of Sn in Ge (<1%), this alloy is thermally unstable, impeding dopant activation after implantation, and thus, hindering the in-plane device fabrication.

In this work, we present the fabrication and characterization of GeSn nanowires grown by CVD-VLS and their use for NWs TFET devices. Growth of single GeSn NWs, in situ doping and p-i-n heterojunction will be investigated.

2. Method and results

Material growth

GeSn nanowire were grown in a hot-wall CVD system (Easytube 3000 from First Nano) on germanium (111) oriented substrate. GeH_4 and $SnCl_4$, were used as precursor for germanium and tin respectively, with N_2 as carrier gaz. The doping modulation of NW is obtained by introducing the dopant precursors, B2H6 and PH3 to p-type and n-type doping respectively. In addition to the other gas precursors, 10 sccm of HCl was used to hinder the 2D uncatalyzed growth and avoid tapering. Gold colloids of calibrated diameters were used as catalyst for the VLS growth.

Results

Since Sn have a low solubility in Ge (<1%), Sn incorporation in the nanowire mostly occur in non-equilibrium system. To overcome this challenge, solute trapping offer the possibility to incorporate high tin amount in the nanowire. This mechanism occur at high crystallization velocity. Hence the growth rate of GeSn nanowire was investigated as a function of the precursors partial pressure for several temperature.

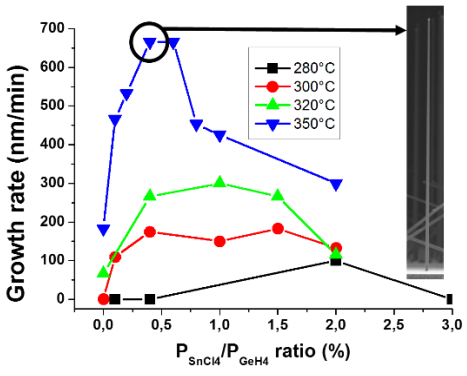

Fig. 1. Growth rate of GeSn nanowire as a function of $SnCl_4/GeH_4$ ratio for different temperature with a typical SEM image of a nanowire grown at 350°C, 0.4% ratio.

One can see that sample grown at 350°C with a 0.4% ratio present the highest growth rate, and thus, potentially the highest Sn incorporation. We

performed physico-chemical analysis such nano-Auger depth profile and STEM EDX (inset) shown in Fig. 2 to quantify the Sn presence.

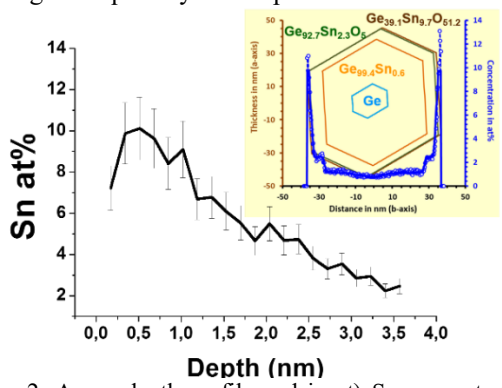

Fig. 2. Auger depth profile and inset) Sn concentration along the nanowire with a cross sectional reconstitution.

The nanowire exhibits a Sn rich shell with up to 10%, rapidly decreasing with a pure Ge core. This spontaneous core-shell formation was attributed to a non-uniformity of the catalyst during the nanowire growth. Since the inversion layer during channel polarization is present at the oxide/SC on few nanometers, the tunneling of carriers will mostly occur in the GeSn shell. Since p-TFET require controlled n^+ doping for the source, phosphorous doped GeSn nanowire were grown.

Hence, five sample in the same condition with additional flux of 100 sccm, 80 sccm, 60 sccm, 40 sccm and 20 sccm of PH_3 were grown in order to investigate the in-situ doping. Dopant incorporation during the NW growth was carried out by resistivity measurements on single GeSn NW using four-probe configuration. Doped nanowires were drop casted on 100nm Si_3N_4 insulator. Conventional photolithography process was used to design a four probe pattern onto an isolated nanowire, then 10 nm of titanium and 90 nm of gold were deposited to form the contacts.

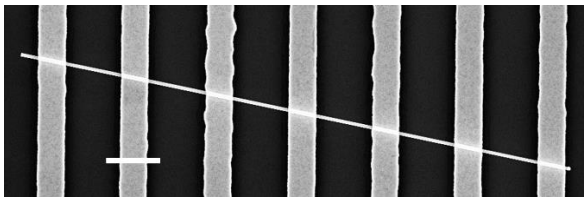

Fig. 3. SEM image of multiple contacts on GeSn nanowire. Scale bar represent 2 µm.

Doping measurement and p-i-n junction will be further presented.

3. Conclusion

We presented the growth and the characterization of single GeSn nanowires realized by CVD-VLS. We demonstrated the feasibility of one step growth p-i-n junction GeSn nanowire in order to realize tunnel FET.

Acknowledgements

The authors would like to thanks the Labex MINOS (ANR-10-LABX-55-01) for financial support.

Reference

[1] Q. Huang *et al.*, "A novel Si tunnel FET with 36mV/dec subthreshold slope based on junction depleted-modulation through striped gate configuration," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 8–11, 2012.

[2] C. Le Royer *et al.*, "Fabrication and electrical characterizations of SGOI tunnel FETs with gate length down to 50 nm," *Solid. State. Electron.*, vol. 115, pp. 167–172, 2016.

[3] S. Takagi, M. S. Kim, M. Noguchi, K. Nishi, and M. Takenaka, "Tunneling FET device technologies using III-V and Ge materials," *2015 4th Berkeley Symp. Energy Effic. Electron. Syst. E3S 2015 - Proc.*, pp. 7–8, 2015.

[4] R. Pandey *et al.*, "Performance benchmarking of p-type $In_{0.65}Ga_{0.35}/GaAs_{0.4}Sb_{0.6}$ and $Ge/Ge_{0.93}Sn_{0.07}$ hetero-junction tunnel FET" in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 19.6.1-19.6.4.

[5] P. Moontragoon, Z. Ikonić, and P. Harrison, "Band structure calculations of Si–Ge–Sn alloys: achieving direct band gap materials," *Semicond. Sci. Technol.*, vol. 22, no. 7, pp. 742–748, 2007.

[6] C. Liu, "Electronic structure and transport calculations of group-IV semiconductors," no. May 2018, 2016.

[7] M. A. Mahjoub *et al.*, "Impact of Wet Treatments on the Electrical Performance of Ge 0.9 Sn 0.1 -Based p-MOS Capacitors," *ACS Appl. Electron. Mater.*, vol. 1, no. 2, pp. 260–268, Feb. 2019.