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388 K High Temperature Retention Study of 2D Hetero-stack Based Non-Volatile Memory

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Abstract: For the first step to build a thermally accelerated retention test for 2D hetero-stack based non-volatile memory (NVM), retention test was conducted over 10^4 s at 388 K. It is revealed that the data loss of both low resistance state (LRS) and high resistance state (HRS) is accelerated at the high temperature, and the HRS is more stable than the LRS even at 388 K. In addition, the 298 K LRS retention characteristics are not linear against time. This means the linear extrapolation could not estimate 10 years retention of 2D hetero-stack based NVM correctly.

1. Introduction

Due to the fundamental limitation of conventional Si based electronics, 2D materials are attracting a lot of attention as a candidate of next generation electronics materials. In particular, non-volatile memory (NVM) which can store the binary 0/1 data without power supply is one of the key components of current electronics systems. Since the superior electrical reliability is expected for the 2D layered structure due to the dangling bond free interface, 2D hetero-stack based NVMs have been studied and their concepts have been demonstrated [1-4]. However, because of the lack of systematic studies on the retention performance, the fundamental understanding on how 2D hetero-stack based NVM is superior to the conventional 3D NVM is quite limited.

In general, 10 years retention is required for NVM. Therefore, the stability based on the thermally accelerated retention test has been intensively discussed for Si system. In this study, for the first step to build the thermally accelerated retention test for 2D hetero-stack based NVM, the retention test was conducted at not only room temperature (298 K) but also high temperature (388 K) for 10^4 s. From the results, it is revealed that the data loss of both states (low resistance state: LRS / high resistance state: HRS) are accelerated at the high temperature and the HRS is more stable than the LRS. Moreover, the current against time characteristics for 298 K LRS retention are not linear. This means more than one degradation mechanism exists in LRS retention and the liner extrapolation does not provide the 10 years retention correctly.

2. Device Fabrication

The schematic diagram and the optical image of 2D hetero-stack based NVM are shown in **Fig. 1**. The exfoliated MoS_2 flake was transferred onto a SiO_2 (~90 nm) / n^+-Si substrate as a floating gate (FG) of the 2D hetero-stack based NVM. The thin *h*-BN as a tunnel barrier and MoS_2 as a channel were also mechanically exfoliated and transferred subsequently onto the FG MoS_2 flake by dry transfer method using alignment system [5]. Then, the source and drain electrodes were patterned by electron beam lithography and Cu/Ni metals were deposited. The thickness of FG MoS_2, *h*-BN and channel MoS_2 are 34.1, 24.5 and 9.99 nm, respectively, which are defined by AFM.

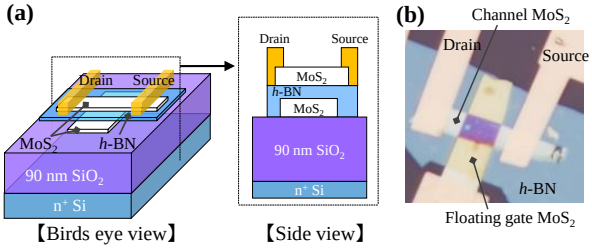

Fig. 1. (a) Schematic diagram and (b) optical image of 2D hetero-stack based non-volatile memory.

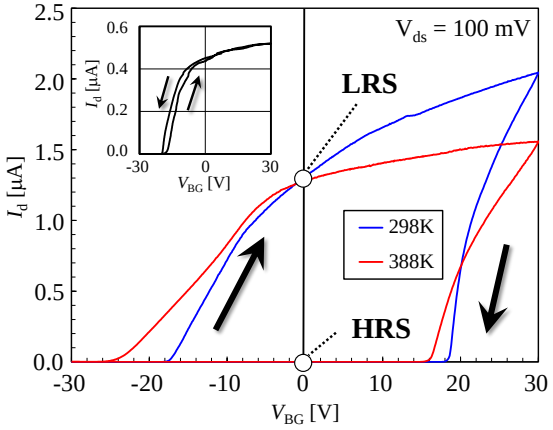

Fig. 2. I_d-V_{BG} curve of the 2D hetero-stack based non-volatile memory The inset shows the I_d-V_{BG} curve with grounded FG at 298 K.

3. Non-volatile memory operation

The I_d-V_{BG} curves of 2D hetero-stack based NVM at 298 K and 388 K are shown in **Fig. 2**. When FG is grounded during the I_d–V_{BG} measurement, as shown in the inset of **Fig. 2**, the size and the direction of hysteresis loop is different from those in the main figure. Since the small hysteresis comes from the orientation polarization due to the adsorbates like water, it is clear that the large hysteresis in the main figure (threshold voltage deference ΔV_{th} > 30 V) attributes to the charge trapping by FG MoS_2. When V_{BG} was swept from -30 V to +30 V, the 2D hetero-stack based NVM reached LRS at 0 V. This means that the potential of FG MoS_2 becomes positive to enhance the electric field from back gate. Similarly, the 2D hetero-stack based NVM reached HRS at 0 V for the V_{BG} sweep from +30 V to -30 V. The potential of FG MoS_2 becomes negative to reduce the electric field from back gate.

4. Retention characteristics

The retention characteristics at 298 K and 388 K are shown in **Fig. 3**. Before the LRS retention test, V_{BG} = -30 V was applied for 5 s. Similarly, before the HRS retention test, V_{BG} = +30 V was applied for 5 s. The data was read as a drain current under V_{BG} = 0 V and V_{ds} = 100 mV iteratively at the predetermined time duration until 10^4 s. **Figure 3(a)** shows

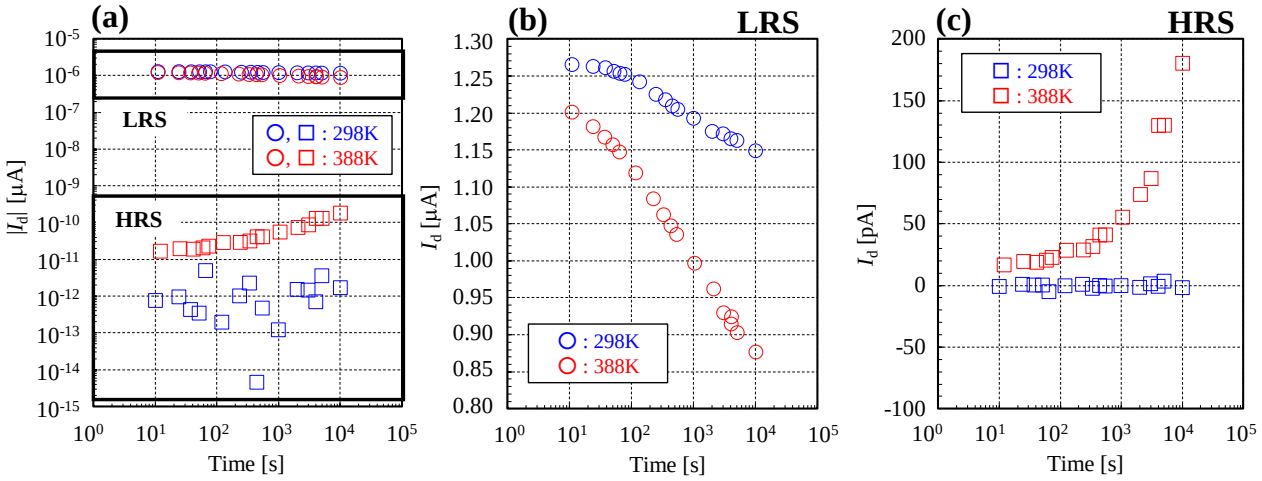

Fig. 3. (a) LRS and HRS retention characteristics of 2D hetero-stack based NVM. The LRS retention characteristics are enlarged in (b) and the HRS retention characteristics are enlarged in (c).

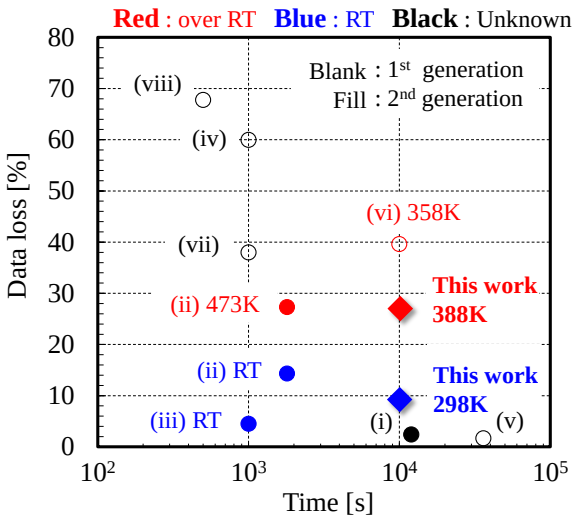

Fig. 4. The data loss of charge trap based three terminals 2D-NVM devices. References are as follows.
(format: HRS or LRS / Metrics / Literature), (i) LRS / I_d / *ACS Appl. Mater. Interfaces* 2018, **10**, 37, 31480., (ii) LRS / I_d / *Nat. Commun.* 2013, **4**, 1624., (iii) LRS / I_d / *Adv. Func. Mater.* 2015, **25**, 7360., (iv) HRS / R_{ds} / *Appl. Phys. Lett.* 2011, **99**, 082109., (v) LRS / I_{ds} / *Appl. Phys. Lett.* 2011, **99**, 113112., (vi) LRS / V_{dirac} / *ACS Nano* 2012, **6**, 9, 7879., (vii) LRS / I_{ds} / *Semicond. Sci. Technol.* 2018, **33**, 034001., (viii) LRS / I_{ds} / *Small* 2018, **14**, 1800319.

the retention characteristics of both LRS and HRS in log scale. The retention characteristics of LRS and HRS are enlarged in linear scale in **Figs. 3 (b) and (c)**, respectively.

It was clearly observed that the data loss was accelerated at the high temperature for both states. For LRS, although the I_d was decreased only 117 nA (9.2%) at 298 K, that was reduced 324 nA (27.0%) at 388 K from 10 to 10^4 s. For HRS, drain current was increased from 16.7 pA to 180.3 pA in 388 K even though no significant current increase was observed at 298 K from 10 to 10^4 s. It was reported that the electron was accumulated in MoS_2 at high temperature by "desulfurization" [6]. However, I_d decreased by several hundred nA in LRS, while it increased by only less than 200 pA in HRS. These results show that the HRS is more stable than LRS even at high temperature. Therefore, in order to improve the retention characteristics of 2D hetero-stack based NVM, LRS retention should be paid more attention than that of HRS.

In addition, **Figure 3(b)** clearly show the LRS retention characteristics in 298 K are not linier against time. It suggests that the more than one degradation mechanism exists in 2D hetero-stack based NVM like Si-based flash memory [7]. Therefore, the linear extrapolation of retention characteristics is not proper to estimate the 10 years retention.

Finally, the "data loss" in previous reports are summarized against time in **Fig. 4**. These data were obtained from charge trap based three terminals 2D-NVM devices. All of them are not extrapolated data but measured data. The "1st generation" refers the device structure in which 2D materials are used only as a channel, and the "2nd generation" refers the device structure in which 2D materials are used as the channel, the tunnel insulator and FG. For the "1st generation" data, the data loss is relatively large, and the variation of data is also large. On the other hand, the data loss is limited to around 10% for the "2nd generation" data at RT. Our data is reasonably good compared with other data. From this comparison, it can be considered that 2D channel itself is not sufficient to obtain the superior non-volatility. Therefore, 2D hetero-stack structure can be better choice. Since the no significant data loss is observed even after 10^4 s by 2D hetero-stack structure, the thermally accelerated retention test is highly required to accurate estimation of 10 years retention and discuss the degradation mechanism.

5. Conclusions

It is revealed that the data loss of both states is accelerated at 388 K and the HRS is more stable than the LRS. It is not correct to estimate the 10 years retention by linear extrapolation because the LRS retention characteristics in 298 K is not linear against a time. To predict the lifetime correctly, the detailed study on thermally accelerated retention test is required.

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References: [1] S. Bertolazzi *et.al.*, *ACS Nano*, 2013, **7**, 3246. [2] M. Sup Choi *et al.*, *Nat. Commun.*, 2013, **4**, 1624. [3] S. G. Yi *et al.*, *ACS Appl. Mater. Interfaces*, 2018, **10**, 37, 31480. [4] Q. A. Vu *et al.*, *Nat. Commun.*, 2016, **7**, 1.[5] Uwanno. T *et.al.*, *2D Mater.*, 2015, **2**, 041002. [6] M. D. Siao *et al.*, *Nat. Commun.*, 2018, **9**, 1442. [7] K. Lee *et al.*, *IEEE Trans. Electron Devices*, 2013, **60**, 1099.