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ReS_2 Based High-k Dielectric Stack Charge-Trapping Memory

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Abstract

The coming information era brings data explosion. In this artical, a ReS_2 based high-k dielectric stack ($Al_2O_3/ZrO_2/Al_2O_3$) memory was fabricated as a potential candidate for future storage. The device exhibits preeminent memory characterics, such as high On/Off current ratio (over 10^6), large memory window (4 V at a 5 V sweep voltage), fast programming and erasing speed plus excellent retention ability, which promising a bright future for our memory device.

1. Introduction

With the development of information ages, data size in various media is explosive. Huge quantity of data requires more storage devices with higher performance and smaller size. Further miniaturization of traditional metal-oxide-semiconductor field-effect transistor (MOSFET) is reaching the limitation [1]. Two-dimensional (2D) materials with atomical thickness are prospective semiconductors for future storage devices. 2D materials such as graphene and transition metal dichalcogenides (TMDs) have been widely explored and they have been demonstrated with excellent optical and electronic properties [2,3]. Most widely researched 2D materials such as MoS_2 and WSe_2 which have symmetric lattice structure showing isotropic electronic properties, while anisotropic TMDs due to distorted lattice structure have been rarely studied. Rhenium disulfide (ReS_2) is a typical anisotropic material with a distorted octahedral (1T) crystal structure [4]. Compared to the other TMDs that a monolayer structure with a direct bandgap and a multilayer structure with an indirect bandgap, ReS_2 within ten layers are all considered to have direct band gap. Therefore, the interlayer coupling energy is much weaker in ReS_2, which makes the monolayer exfoliation much easier and facilitates the fabrication of ReS_2 memory devices.

2. Material characterizations and device fabrication

Fig. 1(a) shows the side and top views of the monolayer ReS_2 crystal structure, wherein adjacent Re (blue) atoms are bonded in the form of zigzag four-atom clusters on account of Peierls distortion. The *a* and *b* arrows, which are 61.03° or 118.97° apart are respectively the second-shortest axis and the shortest axis in the basal plane. Previous studies have testified that the maximum mobility of ReS_2 crystal is along the shortest *b* axis which corresponds to the Re–Re atomic chain direction [5]. The atomic force microscopy (AFM) image of the ReS_2 film is shown in Fig. 1(b), the inset shows that the thickness of the ReS_2 film is about 3.7nm indicating a five-layer ReS_2 film (0.7~0.8nm for a monolayer film). When manufacturing the ReS_2 memory device, direction *b* was selected as the direction of channel current to best display memory properties.

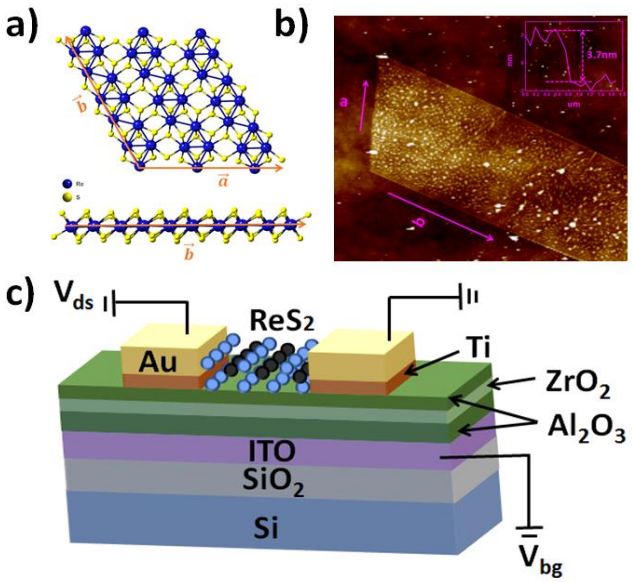

Fig. 1 (a) Crystal structure of monolayer ReS_2 with a top view in the top panel and a side view in the bottom panel. Both directions of *a* and *b* axes are denoted by red arrows. (b) AFM image of a five-layer ReS_2. Inste: the height profile along the pink arrow indicating a 3.7 nm height. (c) Schematic diagram of ReS_2 memory device.

The schematic structure of our ReS_2 memory device is shown in Fig. 1(c), a highly p-type doped Si coated with a 200 nm SiO_2 was used as the substrate. After physical vapor deposition operation, the SiO_2/Si substrate was covered by a layer of 70 nm Indium tin oxide (ITO) film, then annealing them in N_2 for 10 minutes at 400 ℃. The sandwich type $Al_2O_3/ZrO_2/ Al_2O_3$ structure with a 12/4/4 nm thickness was grown on ITO by atomic layer deposition (ALD). Then, a mechanically exfoliated 5-layer ReS_2 film was deposited on the sandwich stack and carpeted with Ti/Au electrodes with a thickness of 10/70 nm. In our ReS_2 memory device, the ITO and Ti/Au layer act as back gate electrode, source and drain electrodes, respectively. Compared to the traditional top gate design which directly deposite the high-k dielectric on the channel materials and cause great damage to TMDs [6], the back gate structure well protects the properties of ReS_2, making sure our device has good performance. The 12-nm thick Al_2O_3 layer acts as a barrier layer, the ZrO_2 and 4-nm Al_2O_3 layer act as electron capture layer, and a tunneling layer, respectively. Since the conduction band of ZrO_2 is lower than Al_2O_3 and the valence band is higher than

Al_2O_3, this sandwich structure can effectively accomplish charge capture and storage.

3. Results and discussion

The output curve displays the drain-to-source current (I_{ds}) which first rises linearly and then becomes saturated when the drain-to-source voltage (V_{ds}) changes from 0 V to 1 V at a fixed back gate voltage, as shown in Fig. 3(a). The excellent saturation characteristics correspond to the strong channel regulation by the ITO back gate electrode. Fig. 3(b) shows four clockwise hysteresis loops at different V_{bg} sweep ranges, the memory window increased from 1 V to 4 V when changing sweep range from ± 2 V to ± 5 V, and the On/Off current ratio is over 10^6 at a 5V V_{bg} swing. These characteristics indicating a typical n-type memory device. The energy band diagram of the device is shown in Fig. 2(c), where it can be seen when applying a positive voltage on the ITO back gate electrode, the energy bands bent in the direction of ITO, and the electrons gathered in the ReS_2 channel tunneled through the Al_2O_3 layer to the ZrO_2 layer. However, negative voltage excited the electrons to move from the ZrO_2 layer to the multi-layer ReS_2, and the energy bands bent in the direction of channel.

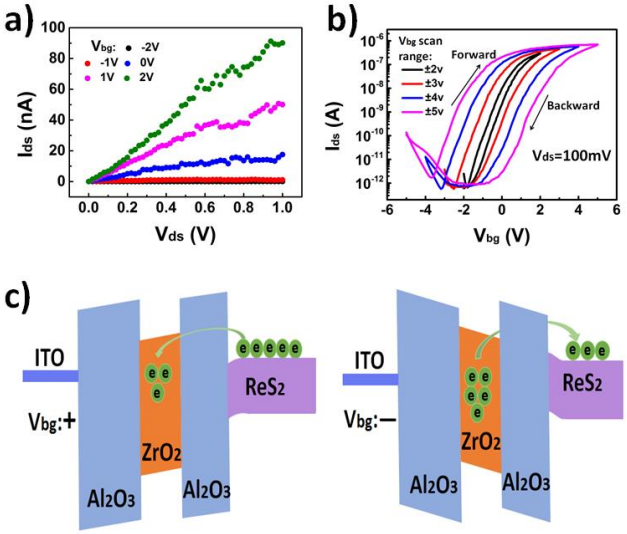

Fig. 2 (a) Output characteristics (I_{ds} –V_{ds}) of the ReS_2 memory device at a fixed V_{bg} changing from -2 V to 2 V with the step of 1 V. (b) I_{ds}-V_{bg} hysteresis loops in different V_{bg} sweep ranges of ±2 V, ±3 V, ±4 V, and ±5 V, respectively. (c) Energy band diagram of the ReS_2 memory devices with positive and negative ITO voltage respectively.

To get a better sense of charge moving, the P/E operations were performed to demonstrate the capture and release of electrons between the ReS_2 channel and the charge-trapping layer. A clear right shift of the I_{ds}-V_{bg} curves can be observed when increasing the programming time. As shown in Fig. 3 (a), a threshold voltage shift (ΔV_{th}) of 1 V was achieved after a 3 V, 1 s programming pulse. Fig. 3 (b) shows erasing characteristics with different erasing time at fixed -3 V back gate pulses. The device demonstrate excellent retention properties after P/E operations (Fig. 3 (c)), the memory window can keep steady for a long time.

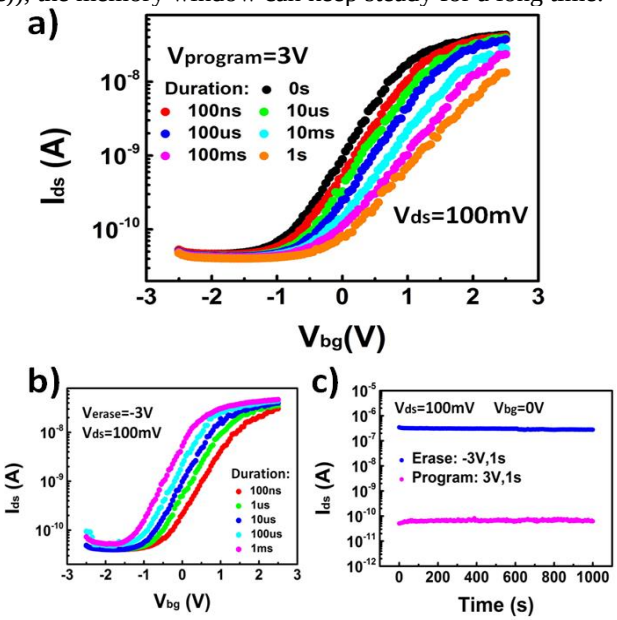

Fig. 3. (a) Programming operations with different pulse duration at a fixed 3 V pulse amplitude. (b) Erasing operations with different pulse duration at a fixed -3 V pulse amplitude. (c) Endurance characteristics of the ReS_2 memory device. The P/E operations were performed by applying 3 V, 1 s and -3 V, 1 s back gate voltage pulses, respectively.

4. Conclusions

In this work, we fabricated a high-k dielectric stack memory device using anisotropic 2D ReS_2 material. The operation voltage of our device with only a 20 nm distance between the ReS_2 channel and the ITO electrode is below 5 V, promising fast P/E speed and low power consumption. Besides, the device showed excellent retention ability. These features enabling our device to be next generation ultra-thin memory device in the futuer.

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