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Electrical characteristics of 2D MoS_2 ferroelectric memory transistor with ferroelectric $Hf_{1-x}Zr_xO_2$ gate structure

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Abstract

We report a back gate ferroelectric memory field-effect transistor with few-layered MoS_2 channel controlled by $Hf_{1-x}Zr_xO_2$ (HZO) ferroelectric gating. The HZO/MoS_2 ferroelectric field-effect transistor (FeFET) exhibits clear counterclockwise hysteresis loop of 4 V induced by ferroelectric polarization domain. The HZO/MoS_2 FeFET shows high on/off current ratio of more than 10^7 and clear counterclockwise memory window of 4 V. The high endurance and the static retention properties are also demonstrated. Thus, our results demonstrate that the HZO/MoS_2 ferroelectric memory transistor can achieve potential use in nano-sized non-volatile memory applications.

1. Introduction

Ferroelectric (FE) materials including lead zirconium titanate (PZT), doped-HfO_2 have been widely used in FeFETs. At the same time, Molyb denum disulfide (MoS_2) have been regarded as promising channel materials for high on/off current ratio (10^8) [1] and environmental stability. Notably, MoS_2 FeFETs with low operating voltages have received great attention recently [2,3]. However, a real ferroelectric controlled HZO FeFET based on MoS_2 channel is rare.

In this work, we proposed a ferroelectric memory transistor based on few-layered MoS_2 and the HZO film. Due to ferroelectric polarization domain, the HZO/MoS_2 ferroelectric memory transistor exhibits clear counterclockwise hysteresis loop. Experimental results demonstrate high on/off current ratio of more than 10^7, clear counterclockwise memory window of 4 V, high endurance and the static retention properties. Thus, the HZO/MoS_2 ferroelectric memory transistors potentially pave a new way for future non-volatile memory devices.

2. Device Fabrication

Fig. 1 displays the schematic view of HZO/MoS_2 FeFET structure. 6 nm $Hf_{1-x}Zr_xO_2$ film and 2 nm Al_2O_3 was deposited on p+ Si substrate using atomic layer deposition (ALD) at 300 ℃. Subsequently, the substrate undergone rapid thermal annealing (RTA) at 450 ℃ for 30 s in N_2. After that, few-layer MoS_2 flakes were mechanically-exfoliated and transferred onto the substrate. Then 5 nm Ti/ 65 nm Au were patterned as the source/drain electrodes by e-beam lithography (EBL) and e-beam evaporation (EBE). Finally, the device was annealed at 300℃ for 2 hours to enhance the contact. Before investigate the characterization of the HZO/MoS2 FeFET, the P-V curve was shown in Fig. 2. We can clearly observed that the coercive voltage of the MIS capacitor is ~3.2 V.

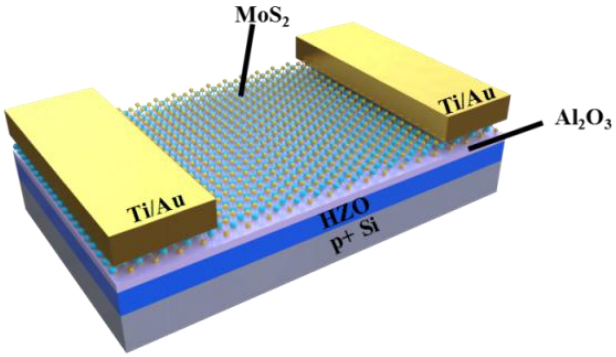

Fig. 1 3D schematic image of the MoS_2 back-gate transistor with ferroelectric HZO gate dielectrics.

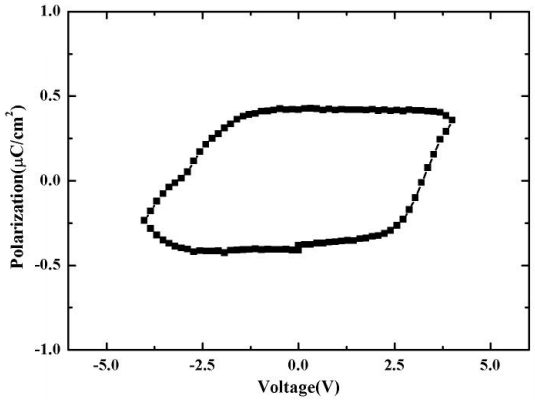

Fig. 2 P-V curve of a Au/HZO/p+ Si MIS capacitors.

3. Device Performance

For different back gate voltage sweep ranges and different drain voltages, the hysteresis loops of the HZO/MoS_2 FeFET were shown in Fig. 3. The hysteresis-free loops in Fig. 3(a) and Fig. 3(b) means that ferroelectric polarization is stifled by charge trapping/detrapping. The hysteresis loops in Fig. 3(c) were counterclockwise when the back gate voltage is swept from -4 V to 4 V and back to -4 V at V_{ds} = 0.4 V. The maximum voltage under the drain is V_g - V_{ds} = 3.6 V, which should be larger than the coercive voltage V_c to switch the ferroelectric at the drain side. The estimated coercive voltage is consistent with PV measurements in Fig. 2. The counterclockwise hysteresis loops in Fig. 3(d) results from the ferroelectric polarization

domination. When the applied voltage in HZO film exceeds the positive coercive voltage, the ferroelectric polarization points into the MoS_2 channel. Therefore, the electron charges in the MoS_2 channel accumulate and the threshold voltage decreases. When the applied voltage in HZO film exceeds the negative coercive voltage, the ferroelectric polarization points away from the MoS_2 channel. Therefore, the electron charges in the MoS_2 channel deplete and the threshold voltage increases. Nonetheless, we observed that a wider back gate voltage range produced a larger hysteresis. This indicates that ferroelectric polarization switching can be enhanced by larger applied voltage, leading to a greater shift in threshold voltage. When the back gate is swept from -6 V to 6.5 V and back to -6.5 V in Fig. 4(a), the counterclockwise memory window width reaches 4 V.

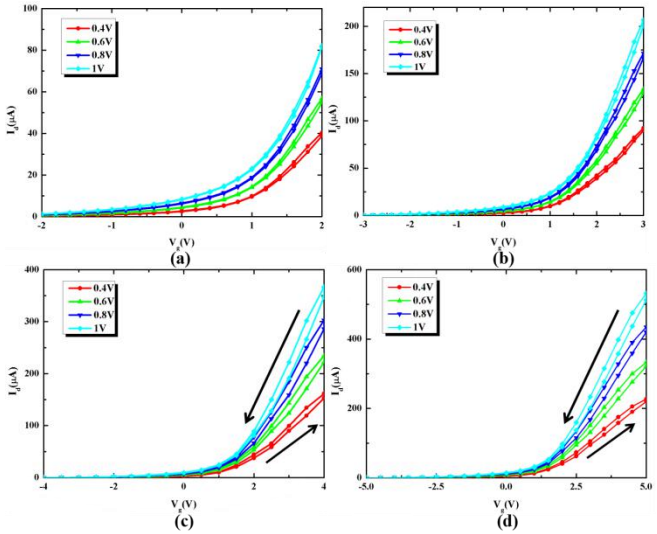

Fig. 3 Transfer curves of the HZO/MoS_2 FeFET at increasing V_g range with linear y-axis.

After the above direct current (DC) test of the HZO/MoS_2 FeFET, we further carried out the measured memory windows (MWs) for different program/erase (P/E) V_g pulses with 10 ms width in Fig. 4(b). MW is defined as the maximum change ΔV_{TH} after P/E V_g pulses. During the pulsed V_g application, the other terminals were fixed to V_s = V_d = 0 V. For reading the MWs, V_g was scanned in the small 1.2 V range with V_d = 0.5 V and V_s = 0 V fixed. As shown in Fig. 4(b), the extracted MWs were larger than 0.2 V when P/E V_g pulses were imposed with ±3 V, ±4 V, ±5 V and ±6 V heights.

Finally we studied the cycling endurance and data retention of the HZO/MoS_2 FeFET. The program V_g pulse was 4 V and 10 ms wide high with V_s = V_d = 0 V. The erase V_g pulse was -4 V high and 10 ms wide with V_s = V_d = 0 V. For the read, V_g was ranged from -1 V to 1 V with V_d = 0.5 V and V_s = 0 V. Fig. 5(a) illustrates the endurance measured up to 10^3 P/E cycles with pulse width of 10 ms. As shown in Fig. 5(b), the memory window increases to 0.26 V after 100 cycles and and then decreases back to 0.19 V after 1000 cycles. The first broaden MW is called "wake-up"effect and the later shrunken MW is called fatigue effect. The "wake-up" effect corresponds to domain-wall de-pinning, leading to the increase of switchable polarization domains of the HZO film. The fatigue effect corresponds to newly injected charges that pin the domain walls after great numbers of program/erase cycles. The data retention at room temperature is shown in Fig. 5(b). Here, the MW degradation is negligible after 10^4 s. Therefore, an MW about 0.2 V can be expected to be sustainable over 10 years by the dotted extrapolation lines.

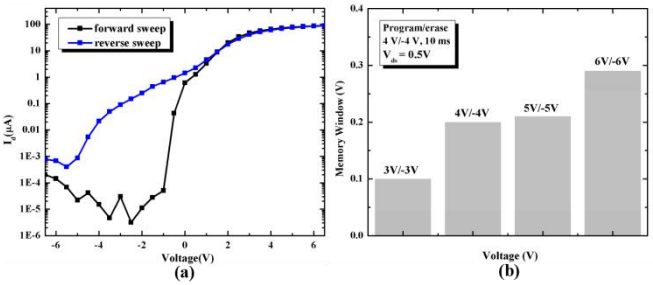

Fig. 4 (a) Transfer curves of the HZO/MoS_2 FeFET with the logarithmic y-axis. (b) Extracted MWs under different program/erase (P/E) conditions.

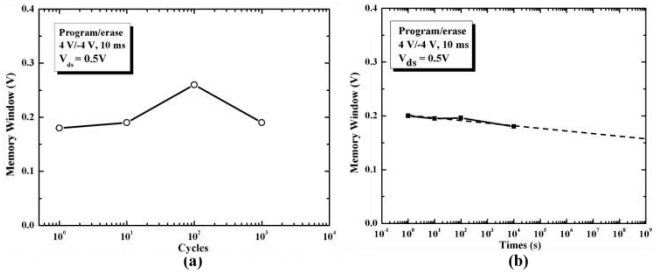

Fig. 5 (a) Endurance measurements under P/E pulse conditions. (b) Retention characteristic of the HZO/MoS_2 FeFET.

4. Conclusions

In conclusion, we developed few-layered, MoS_2-based ferroelectric memory transistor devices using a HZO back gate dielectric. Our fabricated devices exhibit clear counterclockwise hysteresis induced by ferroelectric polarization. In addition, our HZO/MoS_2 ferroelectric memory transistor displayed excellent device characteristics: a high on/off current ratio of more than 10^7, a clear counterclockwise memory window of 4 V, high endurance and the static retention properties. We thus believe that the results of our MoS_2-based nonvolatile ferroelectric memory transistors exhibit promising perspectives for the future of 2D low-power non-volatile memory applications.

References

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