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Engineering superconducting quantum circuits

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Abstract

Superconducting quantum circuits are one of the most advanced platforms for quantum information processing [1], where Josephson junction qubits, with their low dissipation, large nonlinearity, and large dipole moment, play crucial roles [2,3]. Integrated qubit systems aiming at quantum computing are currently developed worldwide. We present our approach to engineered superconducting quantum circuits and discuss their properties.

1. Introduction

It has already been twenty years since the first demonstration of coherent control of a superconducting qubit, an artificial quantum two-level system based on the quantization of collective excitations in a superconducting circuit [4]. Even though the coherence properties looked dauntingly short (~1 ns) initially, the subsequent development in the research field has significantly elongated the time scale by several order of magnitudes. Coherence times of qubits close to or even longer than 100 μs are obtained routinely in many groups nowadays [5]. Thanks to the improvement, perspectives towards quantum information processing on superconducting qubits have been broadly shared [1] and have triggered world-wide research activities. There have been a number of reports on integrated superconducting qubits and basic quantum information processing conducted on small-scale superconducting circuits [6-12]. While the earlier works were mostly on one-dimensionally integrated qubit systems, recently there are more efforts on scaling up in two-dimensional (2D) layouts [13-15]. Here we present our approach towards 2D integration of superconducting qubits.

2. Integrated superconducting qubits for quantum computing

Currently we are developing a 2D integration scheme for superconducting qubits. The design principles are the following: (i) For better coherence and minimal complexity, use fixed-frequency qubits. (ii) Accordingly, use only microwave pulses for control and readout of the qubits. (iii) Minimize the number of wirings per qubit. (iv) Minimize the crosstalk of the control and readout signals. (v) Make the design scalable simply by repeating a unit cell structure.

Our present strategy for fulfilling the requirements is summarized in the following: (i) A 2D square lattice of single-junction concentric transmons capacitively coupled to the nearest-neighbor qubits. The neighboring qubits are frequency-detuned so that their off-state residual coupling is negligible. (ii) Microwave pulses for control and readout are supplied vertically via coaxial cables from the backside of the qubit chip. Impedance-matched spring contacts ensure the connections to the chip. A control line couples capacitively to each qubit. (iii) Single-qubit gates are driven by a resonant Rabi pulse. Two-qubit gates are implemented with a cross-resonance gate, i.e., by driving a qubit with the resonance frequency of the neighboring target qubit [16]. (iv) For the readout, each qubit couples capacitively to an on-chip readout resonator detuned from the qubit. A dispersive readout scheme through the reflection measurement of the readout resonators is used [17]. Four of the resonators in a unit cell consisting of four qubits couple to a Purcell-filter resonator which is capacitively coupled to a superconducting via through the silicon substrate and connected to a coaxial cable. The resonance frequencies of the four resonators are distributed in the bandwidths of the Purcell filter and the following Josephson parametric amplifier so that simultaneous multiplexed readout of the four qubits can be conducted. (v) To suppress the crosstalk of control and readout signals between neighboring qubits and resonators and to suppress any spurious microwave resonances, a number of superconducting through silicon vias connect ground planes on the top and bottom surface of the chip. A cover chip metalized with a superconducting film and flip-chip-bonded on top of the qubit chip is also utilized for eliminating the box modes in the package. The whole chip is enclosed in a light-tight superconducting package to which the backside of the chip is pressed firmly.

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