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300 mm silicon quantum computing: A Silicon-Based Platform for Quantum Computing Device Technologies

S. Kubicek, B. Govoreanu, J. Jussot, BT Chan, N. Dumoulin-Stuyck[1],
F.A. Mohiyaddin, R. Li, G. Simion, Ts. Ivanov, J. Lee, I.P. Radu

imec, Kapeldreef 75, B-3001 Leuven, Belgium
[1]*also with* KU Leuven, Kasteelpark Arenberg 10/44, B-3001 Leuven, Belgium

Email: kubicek@imec.be

Abstract

Flexible 300mm-production-compatible integration platform for exploring the fundamental concepts of Si-MOS quantum computing devices is discussed. The process is based on combination of optical and e-beam lithography which provides the flexibility in exploring different device concepts in terms of layout, integration, processes and materials.

1. Introduction

A great progress in Quantum Computing (QC) has been achieved since the birth of the idea in early 1980s [1]. Among many potential physical qubit implementations in the solid state, the most promising candidates are superconducting (SC) and semiconducting spin-based qubits. There are already demonstrations of small-scale quantum computers with several SC qubits [2] while fulfillment of all necessary requirements posed on the qubit candidates by the DiVincenzo criteria [3] were already demonstrated for semiconducting spin qubits [4,5,6,7,8]. Because of the many similarities between SC and semiconductor spin-based qubits and advanced CMOS process, QC started to attract research by semiconductor manufactures [9,10]. It is hoped that use of most advanced manufacturing techniques will contribute to further progress in QC. IMEC QC research is focusing on both the above-mentioned solid-state qubit candidates. Very few prototypes of silicon qubits have been demonstrated so far, mostly based on academic research with low yield. Hence, it is crucial to explore different device geometries, critical dimensions and materials, and identify devices that yield optimal qubit performance. This would require a flexible fabrication strategy that allows us to scan different device variations. We have developed a simple yet flexible integration platform, which, while using the most advanced processing techniques in the state-of-the-art 300mm cleanroom, provides universality in exploring different device concepts regarding qubits device structures, qubit manipulation, qubits interactions and readout. In this paper, we report the fabrication workflow and preliminary measurements on silicon spin-based qubits. The objective is to use this platform to gain sufficient understanding of spin qubits and develop full qubit models and characterization procedures from room temperatures down to cryogenic (~ tens of mK) temperatures while gradually extending this work to full CMOS technology node for the final co-integration of qubit and control circuitry.

2. Process and design

We have chosen to work with the qubits based on the electron spin of a single electron trapped in Si-MOS based Quantum Dots (QD) by means of applying confining electrical potential to system of the gates, like in Ref. [4]. The electrons in the quantum dots are populated from an electron-reservoir, defined electrostatically from a reservoir-junction. A Single Electron Transistor (SET) adjacent to the quantum dots can be used as the charge sensor for qubit readout. Electron spin manipulation is either through the Electron Spin Resonance (ESR) technique using on-chip ESR micro-wave line or electric dipole spin resonance (EDSR) technique using on chip Cobalt micromagnets. The qubit-to-qubit interaction is based on the exchange interaction of electrons in neighboring QDs. The process flow schematic is presented in Fig.1.

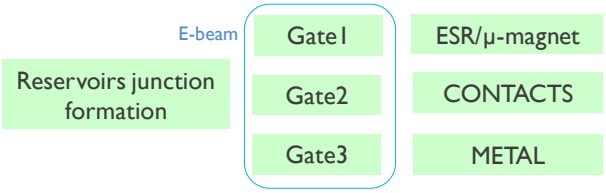

Fig.1 Schematics of the experimental process flow

The process starts with the creation of reservoir junctions by means of standard ion-implantation and anneal. The system of three levels of nested MOS gates is then fabricated. The ESR line or micromagnets are then realized.

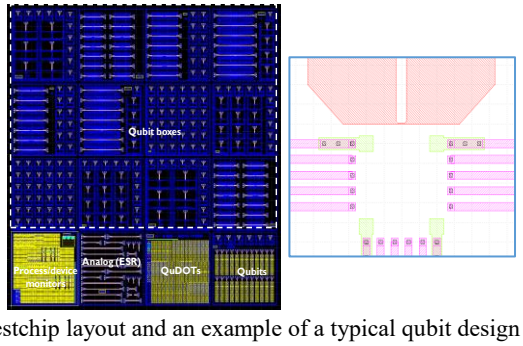

Fig.2 Testchip layout and an example of a typical qubit design box.

The flow is completed by simple contact and metallization modules, enabling bonding. All non-critical levels are patterned by DUV optical lithography, while the three gate levels are patterned by means of a VSB+CP 50kV Acceleration voltage Advantest F7000S ebeam tool. Testchip design features concept of “qubit design boxes” i.e. all the device parts

for which only non-critical lithography is required are defined in the optical masks and free space is left for the three e-beam gate levels, see Fig.2. This allows for a great flexibility in modifying the device design. Next to the qubits, testchip design includes all necessary inline physical and electrical characterization test structures which are used for the evaluation of all important physical and electrical characteristics.

The integration platform can be in principle further enhanced by adding a simple FIN module, prior to the fabrication of gates. This would allow for the exploration of alternative quantum dot structures, where electrostatic confinement is partly replaced by geometrical confinement, possibly reducing the number of gates per qubit and opening up paths for up-scalability.

The development was done on standard Si-substrates but the substrates with isotopically purified ^{28}Si are foreseen later for the device studies.

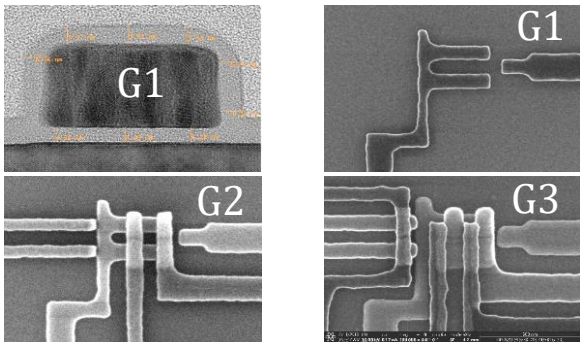

Fig.3 TEM and top-down SEM images of TiN gates

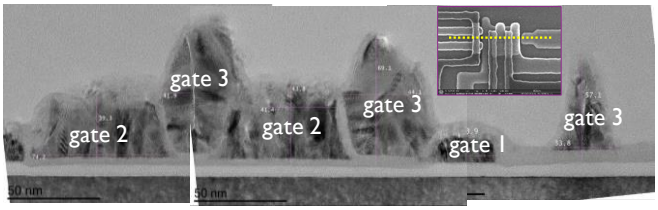

Fig.4 TEM across indicated line (insert) showing system of three levels of nested gates.

Fig.3 and Fig.4 presents illustrative TEM and SEM images of the different gates.

The most critical qubit device region is the interface between the gate dielectric and silicon interface. Imperfections such as defects, atomic roughness and strain at this interface affect the qubit performance. In our studies we have used TiN and Phosphorus doped amorphous silicon as the gate materials, thermally grown SiO_2 as the gate dielectric and ALD SiO_2 or Al_2O_3 as inter-gate dielectrics. To mitigate the negative effect of the interface even more, along with minimizing the strain experienced by the qubits, electron qubits in SiGe/Si/SiGe Quantum Well ~30nm away from the interface, similar to [11], are also being prepared.

In addition to the dielectric/silicon interface imperfections, it was identified that mechanical strain originating from the gate material plays very important role in the operation of qubits [12]. The strain developed in the device region when cooling down to cryogenic temperatures depends clearly on the thermal expansion coefficients of the materials used. This strain results in an unpredictable variation of device electrostatic potential governing qubit behaviour. 2D strain simulations shown in Fig.5 indicate that much more strain is present in Si when TiN is used as the gate material compared to poly Si.

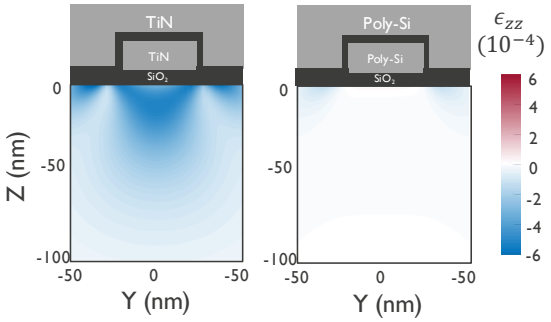

Fig.5 ε_{zz} strain component simulation for the 2 choices of the gate material, TiN and poly Silicon.

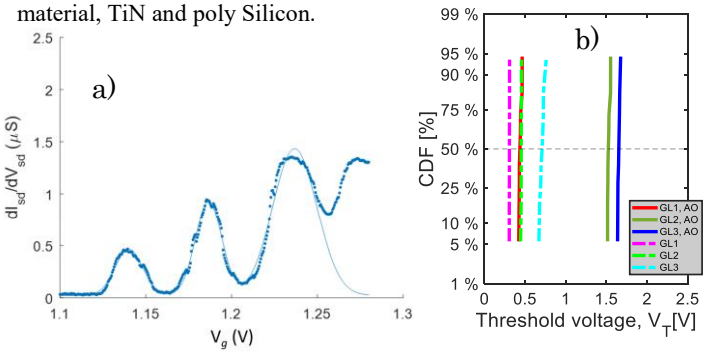

Fig.6 a) Coulomb oscillations measured on our devices at 1.6K and b) cumulative distribution of transistor V_T for SiO_2 and Al_2O_3.

Fig.6 a) shows an example of Coulomb oscillations measured across the SET part in our structure composed of TiN gates and Fig.6 b) CDF of transistor V_T for SiO_2 and Al_2O_3.

3. Conclusions

A simple and flexible device/integration platform for investigating the fundamentals of electron spin-based Si qubits is presented. The platform uses combination of optical and e-beam lithography, and provides the combined advantages of flexibility along with fabrication speed.

Acknowledgements

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