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High Carrier Mobility Sn-Doped Ge Thin-Films (≤ 50 nm) on Insulator by Interface-Modulated Solid-Phase Crystallization at Low-Temperature

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Abstract

Effects of introduction of a-Si under-layers on solid-phase crystallization of Sn-doped Ge on insulator have been investigated. By introduction of a-Si under-layers, energy barrier for carriers at grain-boundaries is significantly decreased. As a result, high carrier mobility of 200−300 cm^2/Vs is realized for thin GeSn films (30−50 nm) grown with a-Si under-layers. This mobility is the highest among ever reported data for Ge and GeSn thin-films (≤50 nm) on insulator grown at low-temperatures (≤500°C).

1. Introduction

Development of a low-temperature (≤500°C) formation technique of high carrier mobility Ge films on insulator is essential to fabrication of high-performance thin-films transistors [1]. Here, the Ge film thickness should be below ~50 nm to achieve fully-depleted devices for high-speed operation with low-power consumption.

Previously, we comprehensively investigated solid-phase crystallization (SPC) of Sn-doped a-Ge films (thickness: 30−500 nm) on insulator (fused-quartz substrates) and clarified that Sn-doping with 2% significantly improves carrier mobility of the grown films, which results in high carrier mobility (320 cm^2/Vs) for thickness of 200 nm [2]. Recently, Imajo et al. investigated densification of pure a-Ge on GeO_2-coated substrates by substrate heating during Ge-deposition and obtained high carrier mobility (620 cm^2/Vs) for thickness of 500 nm [3].

However, in these previous studies, mobility was still degraded near insulating substrates (<120 nm) [2]. This suggests crystal grains initiated from interface-nucleation still degrade the mobility. Thus, the mobility is expected to be further improved by suppressing interface-nucleation. Here, interface-nucleation can be modulated by changing surface energies of substrates. In the present study, we investigate effects of introduction of a-Si under-layers into a-GeSn/substrate interfaces.

2. Experiments and Results

In the experiment, a-Si (thickness: 0−20 nm) and a-GeSn layers (Sn concentration: 2%, thickness: 30−200 nm) were deposited on fused-quartz substrates using a molecular-beam deposition system (base pressure: ~5×10^{-10} Torr). The sample structure is schematically shown in Fig. 1.

Electrical properties and grain structures of grown GeSn layers were analyzed by Hall effect and electron backscattering diffraction (EBSD) measurements, respectively.

Hall effect measurements indicated p-type conduction for all samples, which was attributed to vacancy-related acceptor levels in Ge [2]. Mobility and grain sizes in grown films (GeSn thickness: 50 nm) are summarized as a function of the Si thickness in Fig. 1. The mobility of samples with a-Si under-layers (thickness: 3−20 nm) becomes higher (280−300 cm^2/Vs) compared with that without a-Si under-layer (~220 cm^2/Vs). On the other hand, the grain sizes are significantly decreased by introduction of a-Si under-layers, as shown in Fig. 1. Here, EBSD analysis indicated that preferentially-(100)-orientated grains for the sample without a-Si under-layer change into randomly-orientated grains. This phenomenon is attributed to that preferentially-oriented interface-nucleation is suppressed by introduction of a-Si under-layers, which makes randomly-oriented bulk-nucleation dominant. Interestingly, these results suggest that randomly-oriented small-grain films of samples with a-Si under-layers show higher mobility than the preferentially-orientated large-grain film of the sample without a-Si under-layer.

Figure 2 shows Arrhenius plot of $\mu T^{1/2}$ for grown films, where μ is the mobility and T the absolute temperature. Respective data are well fitted with straight lines. From the slopes of these lines, energy barrier height E_B and trapping state density Q_t at grain boundaries are evaluated using Seto's model [4]. E_B and Q_t are summarized as a function of the a-Si under-layer thickness in Fig. 3. E_B for the sample without a-Si under-layer is ~10 meV. The values are significantly decreased to ~5 meV by introducing a-Si under-layers. The figure also shows that Q_t is decreased from ~6×10^{11} to ~4×10^{11} cm^{-2} by introduction of a-Si under-layers. These findings reveal that mobility improvement by introduction of a-Si under-layers is caused through significant decrease in energy barrier heights at grain boundaries due to decrease in trapping state densities. Since bulk-nucleation becomes dominant over interface-nucleation by introduction of a-Si under-layers, as revealed from the EBSD analysis, these results suggest that boundaries of crystal grains initiated from interface-nucleation show higher density of trapping states compared with bulk-nucleation.

We investigate GeSn thickness dependence of electrical properties and crystal structures. Mobility of samples (Si thickness: 5 nm) is summarized as a function of the GeSn thickness in Fig. 4, together with the grain sizes evaluated by EBSD. With decreasing thickness from 50 to 30 nm, mobility decreases from ~300 to ~200 cm^2/Vs, where the grain sizes hardly change. The decrease in the

mobility is attributed to carrier scattering near the interface. On the other hand, for thicknesses exceeding 50 nm, bulk-nucleation is significantly increased, and thus grain sizes are significantly decreased. This results in the low mobility, as shown in Fig. 4.

Figure 5 shows mobility obtained in the present study, comparing with literature data for Ge and GeSn on insulator grown at low temperatures (≤500°C) [2,3,5,6], as a function of film thickness. Thin films (≤50 nm) are requires to realize fully-depleted devices. Figure 5 shows that the present technique provides the highest mobility among ever reported data of thin films (≤50 nm).

3. Conclusion

Interface-modulated SPC of Sn-doped Ge is investigated. By introduction of a-Si under-layers, interface-nucleation is suppressed, and bulk-nucleation becomes dominant. This reduces energy barrier height at grain-boundaries. As a result, GeSn thin-films (30−50 nm) having a very high mobility (200−300 cm^2/Vs), which is the highest among ever reported data of Ge and GeSn on insulator grown at low-temperatures (≤500°C), are achieved. This technique will facilitate advanced fully-depleted devices for next-generation electronics.

References

[1] M. Miyao et al.,. JJAP **56**, 05DA06 (2017), [2] T. Sadoh, et al., APL **109**, 232106 (2016), [3] T. Imajo, et al., APEX **12**, 015508 (2019), [4] J. Seto, JAP **46**, 5247 (1975), [5] K. Toko, et al., SSE **53**, 1159 (2009), [6] R. Yoshimine, et al., APEX **11**, 031302 (2018).

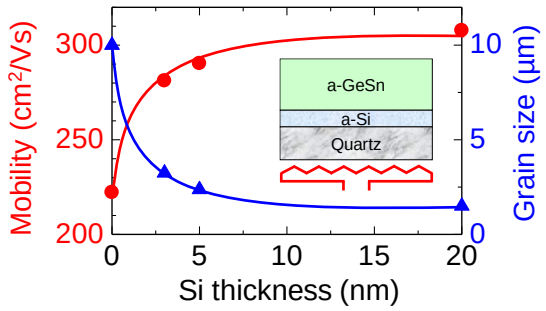

Fig. 1. Schematic sample structure and Si under-layer thickness dependence of carrier mobility and grain size of samples (GeSn thickness: 50 nm) after annealing (450°C, 20 h).

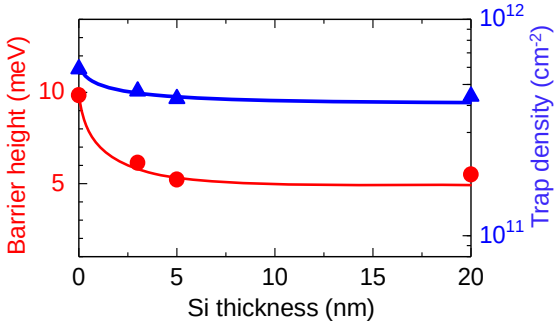

Fig. 3. a-Si under-layer thickness dependence of energy barrier height and trapping state density at grain boundaries for samples (GeSn thickness: 50 nm) after annealing (450°C, 20 h).

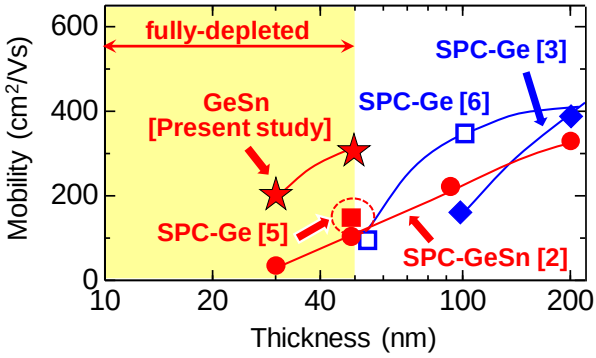

Fig. 5. Mobility obtained in the present study compared with those reported for SPC of pure a-Ge [3,5,6] and a-GeSn (Sn concentration: 2%) [2].

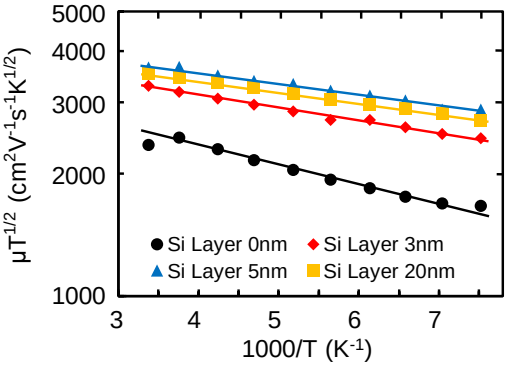

Fig. 2. Arrhenius plot of $\mu T^{1/2}$ for samples (GeSn thickness: 50 nm) after annealing (450°C, 20 h).

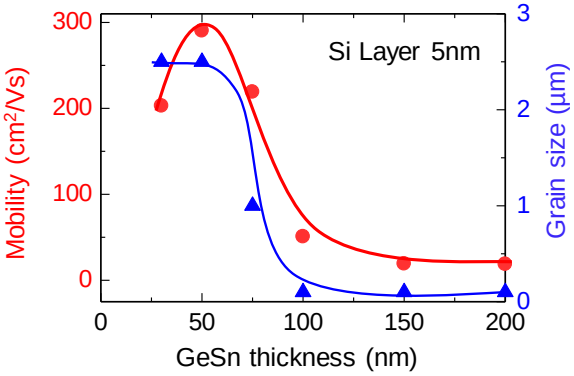

Fig. 4. GeSn thickness dependence of carrier mobility and grain size for samples (Si thickness: 5 nm) after annealing (450°C, 20 h).