Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp301-302

Characteristics of Scaled CAAC-IGZO FET and Its Application to LSI

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Abstract

FETs using *c*-axis aligned crystalline (CAAC) indium-gallium-zinc oxide (IGZO) for channels (CAAC-IGZO FETs) have an extremely low off-state current, specifically, 2.5e−18 A/μm at 150°C when the channel length is 21 nm. Moreover, the CAAC-IGZO FETs enhance their on-state current and cutoff frequency (f_T) as the temperature rises. Especially, a CAAC-IGZO FET with a scaled channel length of 21 nm exhibits f_T = 40 GHz at 150°C. The threshold voltage variation (σ = 35 mV) and +GBT reliability (FET lifetime exceeding 1200 hours at 150°C) of CAAC-IGZO FETs are within a practical range for LSI products. LSI with monolithically stacked Si FETs and CAAC-IGZO FETs has a possibility of application to power-saving logic, memory, analog, and RF circuits which are unfeasible with Si LSI.

1. Introduction

The amount of data to be processed has increased along with upsurges of AI, IoT, and 5G, which generates a demand for high-speed low-power LSIs across all layers of the network, both in from the cloud and at the edge. To meet the demand for low-power LSIs, LSIs with FETs using oxide semiconductors have been studied [1–5]. This study shows the characteristics of CAAC-IGZO FETs whose channel length is 60 nm or less, and the application of the CAAC-IGZO FETs to LSI.

2. Characteristics of Scaled CAAC-IGZO FET

A crystalline structure named CAAC-IGZO, where *c*-axes are aligned, was discovered in 2009. The structure is different from amorphous, single-crystal or polycrystal structures [6]. Using CAAC-IGZO for a channel, we have fabricated a prototype of scaled CAAC-IGZO FET with a top-gate self aligned (TGSA) structure where side surfaces of the channel is covered with the gate as shown in Fig. 1 [7]. This structure enables extremely low off-state current even when the CAAC-IGZO FET is scaled down to have a 21-nm channel. According to evaluation of a test device using the CAAC-IGZO FET to monitor a voltage change of a storage capacitor [8], the leakage current from the drain at 150°C was just 2.5e−18 A/μm as shown in Fig. 2.

The CAAC-IGZO FET is provided with a back gate [9], which enables the control of threshold voltage without changes of transconductance and subthreshold swing (*S.S.*), as shown in Fig. 3. Using CAAC-IGZO FETs allows a high degree of freedom in circuit design, such as fine-grained control of threshold voltages, and dynamic control of threshold voltages [3].

Figure 4 shows temperature dependence of electric performance of CAAC-IGZO FETs [7]. As the temperature rises, *S.S.* becomes large, and the on-state current increases. The former behavior is similar to Si FETs, but the latter behavior is not. As shown in Fig. 5, the Hall mobility of a CAAC-IGZO film increases as the temperature rises. This suggests that Coulomb scattering is more dominant than phonon scattering in CAAC-IGZO's mobility.

The cutoff frequency f_T, which is an important parameter in RF application, also increases as the temperature rises [7]. According to Fig. 6, a scaled FET (L/W = 21 nm/ 25 nm) exhibits f_T = 40 GHz at 150°C. This is a practical value for application to RF because the difference from Si FET's f_T value is just a several times.

Variation in performance and reliability of devices are critical for high-volume manufacturing. According to Fig. 7, CAAC-IGZO FETs have a variation σ in V_{sh} (a gate voltage when the drain current is 1 pA at 1.2 V of a drain voltage) of 35 mV [10]. According to Fig. 8 showing results of plus gate bias temperature (+GBT) testing with a stress temperature of 150°C, V_{gs} = 3.63 V, and $V_{ds} = V_{bs}$ = 0 V, $|V_{sh}|$ does not change more than 100 mV even after 1200 hours [10]. These results indicate that in both the variation in device performance and the reliability, CAAC-IGZO FETs have high durability for practical use in LSI.

3. Application to LSI (OSLSI)

As described above, LSI application of CAAC-IGZO FETs having unique performance has been studied. Memory and normally-off systems using extremely low off-state current of CAAC-IGZO FETs are promising applications for low-power IoT [1–3]. According to the estimates of memory performance based on CAAC-IGZO FET performance [10], the device would be capable of both write time less than 2 ns which corresponds to random access at 200 MHz and retention time more than 1 hour within a temperature range from 85 to −40C°, as shown in Fig. 9. In addition, CAAC-IGZO FETs can be fabricated in the back end of line after fabrication of Si FETs. Utilizing this feature, a circuit using CAAC-IGZO FETs can be stacked over a Si circuit, which enables 3D circuit configuration [4, 5]. By this, application to low-power AI accelerator (Fig. 10) is also expected.

The above application usually requires analog data storage and high writing endurance, which existing nonvolatile memory technologies are difficult to satisfy. Meanwhile, CAAC-IGZO FETs will be promising device to meet the requirements without data degradation because data rewriting is done just by turning on and off CAAC-IGZO FETs, and there is substantially no limit of writing cycles as shown in Fig. 11.

4. Conclusions

CAAC-IGZO FETs exhibit exceptional thermal behavior and cutoff frequency, as well as extremely low off-state current, which enable its scaling down to L = 21 nm and 3D integration with Si FETs and offer a potential of opening the door to novel LSI. Thus, CAAC-IGZO FETs have a possibility of application to novel low-power IoT, AI accelerator, and 5G which are unfeasible with Si LSI.

References

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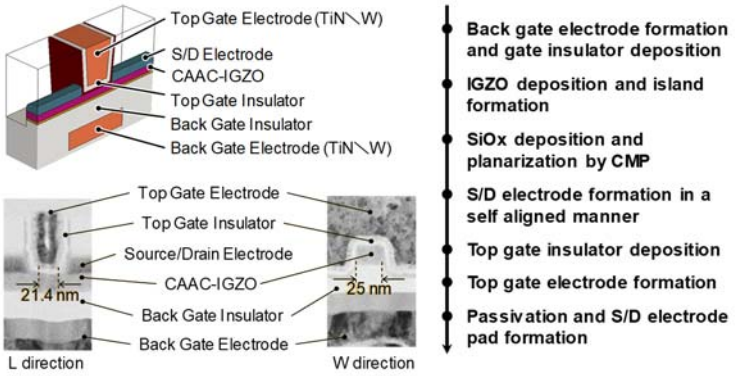

Fig.1 CAAC-IGZO FET structure and its fabrication flow chart.

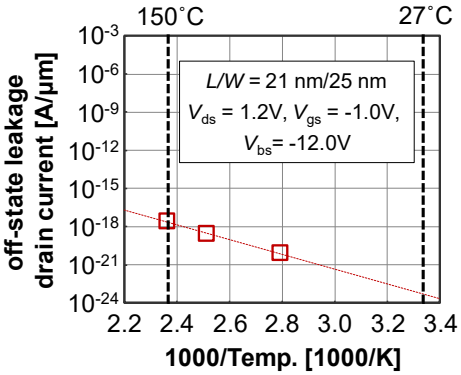

Fig.2 Leakage current of CAAC-IGZO FET.

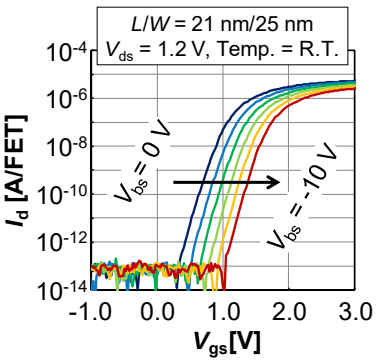

Fig.3 Dependence of *I-V* curves on back-gate voltage V_{bs} of CAAC-IGZO FETs.

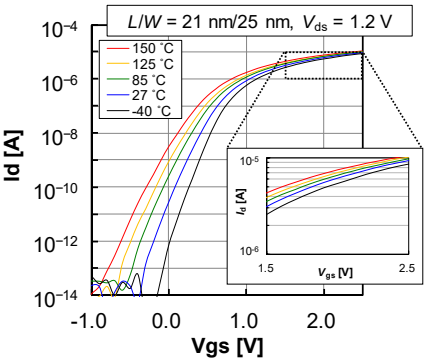

Fig.4 Dependence of *I-V* curves on temperatures of CAAC-IGZO FETs.

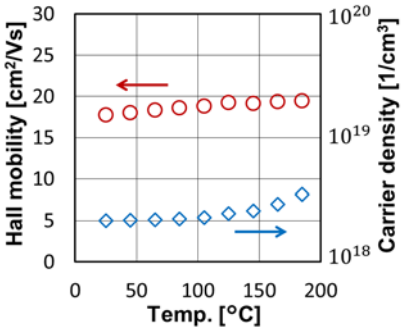

Fig.5 Hall mobility and carrier density of CAAC-IGZO.

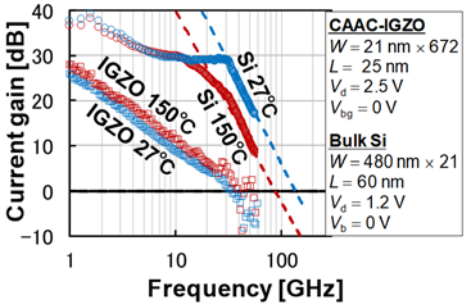

Fig.6 Cutoff frequencies of CAAC-IGZO FETs and bulk Si FETs.

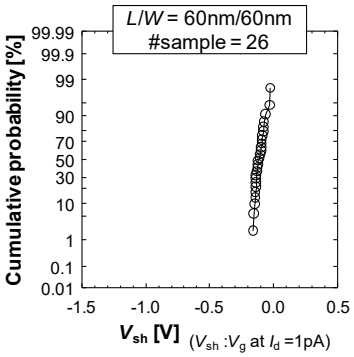

Fig.7 V_{sh} plots of CAAC-IGZO FETs.

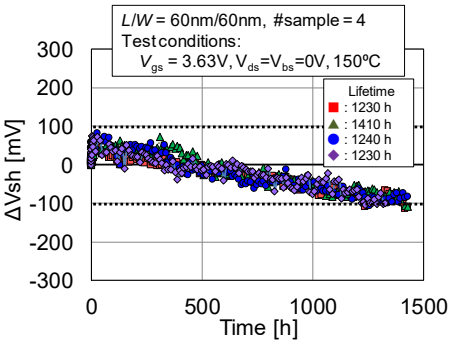

Fig.8 Results of +GBT testing of CAAC-IGZO FETs.

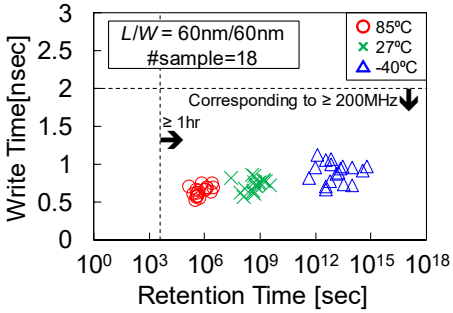

Fig.9 Estimates of operating frequency and retention time.

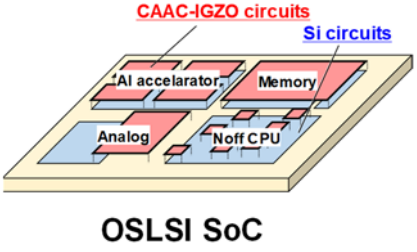

Fig.10 Conceptual diagram of SoC with 3D circuit where Si FETs and CAAC-IGZO FETs are stacked.

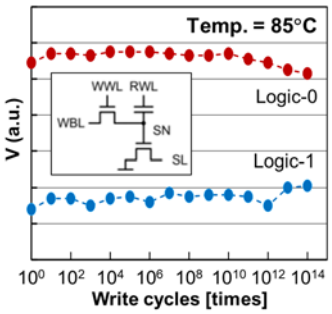

Fig.11 Endurance measurement results of 1-bit memory cell.