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IGZO Integration Scheme For Enabling IGZO nFETs

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***Abstract*—Using Back-gated integration scheme, we demonstrate 130nm IGZO based nFETs. The devices are fully fabricated on 300mm wafers using both amorphous IGZO (a-IGZO) and C-Axis Aligned Crystalline IGZO (CAAC-IGZO or c-IGZO). We achieve maximum measured mobility of 25cm^2/Vs with an I_{on}/I_{off} ratio of approximately 7 decades. With this electrical performance, and by keeping the thermal budget in BEOL compatible range, these devices show high potential for future logic [1] and memory [2] applications.**

1. Introduction

IGZO based thin-film transistors (TFTs) are getting more attention in recent years due to their high mobility, extremely low off current, low process temperature, and good uniformity [3]. In this work, we present a generic process module for enabling IGZO nFETs which is done fully in 300mm FAB, where we show integration scheme for Back-gated IGZO device fabrication. In addition, we also compare electrical performance of a-IGZO and c-IGZO.

2. IGZO device fabrication

Our Back-gated IGZO nFET consists of two main modules, IGZO Active area module (forming the FET channel), and contact module (forming source and drain contacts). Highly doped Si wafer serves as a common back-gate for the transistors. On top, 5nm of PECVD SiCN is deposited, followed by 15nm of ALD Al_2O_3, which serves as gate dielectric. Next step is Pulsed DC PVD IGZO deposition using an AMAT Endura® platform. Next, 180nm of PECVD SiO_2 is deposited which serves as a patterning hard mask (HM). The litho stack for Active area patterning consists of standard SOC/SOG/PR sandwich. The full patterning sequence (except for PR develop and SOC/SOG opening) is shown in Fig 1.

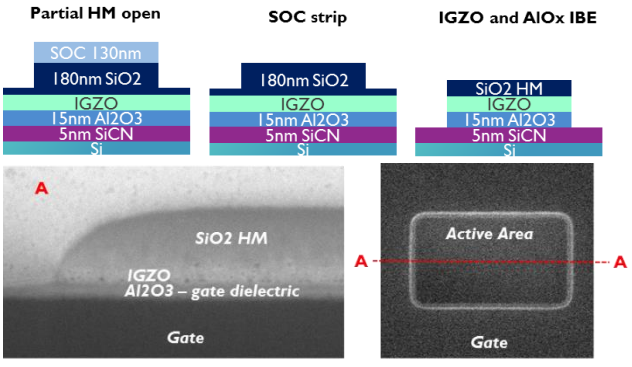

Fig. 1 Schematic cartoon of IGZO Active area formation and Top Down (TD) SEM of the Active Area.

After SOC has been opened, SiO_2 HM is patterned using fluorine-based chemistry. The HM is not fully opened, in order to prevent any IGZO exposure to the etch chemistry. Approximately 30nm of SiO_2 remains after this patterning step. SOC is then stripped using an in-situ O_2 plasma and followed by a wet clean. After partial HM opening, IGZO and gate dielectric are patterned using Ion Beam Etch (IBE). Active area patterning is followed by an additional IBE clean to remove any residues remaining on the top of the Active area. This patterning approach has proven to be very robust, and remains the same, independent on IGZO phase thickness, or the gate dielectric underneath. After the active area has been formed, PECVD SiO_2 is deposited and planarized. Source and Drain contacts are then patterned landing directly on IGZO, where high etch selectivity is maintained. Metallization consists of 20nm PVD TiN (without soft sputter or reactive plasma preclean to limit the possibility of X-contamination) and ALD/CVD W, followed by CMP. Total recess into IGZO after contact formation is ~2nm. Full process sequence of contact formation can be seen in Fig. 2, along with TEM/EDS images of the cross section, and under the contacts.

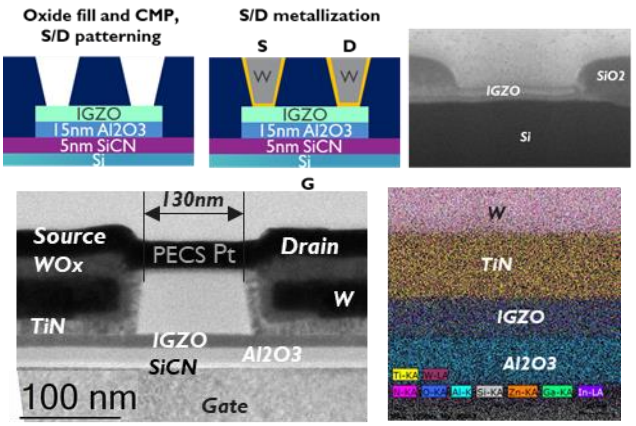

Fig. 2 Schematic cartoon of contact formation for Back-gated IGZO nFET, SEM after contact patterning, and TEM of the final device with L_g of 130nm with EDS map of IGZO under the contacts.

We found that a crucial step for enabling functional IGZO nFETs is a 1hr anneal at 350 °C in pure O_2 atmosphere. Prior to this anneal the IGZO channel is in a highly conductive phase, making device modulation difficult (very negative threshold voltage V_{th}). Additional important aspect when introducing IGZO in 300mm FAB is contamination due to Zn content. While Zn itself is easily cleaned, due to high risk of X-contamination and detrimental impact on Si devices, we classify IGZO as level 3, or BEOL material (such as Cu), where standard BEOL processing rules apply (e.g. mandatory cleans during processing, with addition of TXRF monitoring).

3. IGZO device assessment

As a first screening, we tested a wide range of devices (varying L_g), utilizing 24nm thick a-IGZO, as shown in Fig 4.

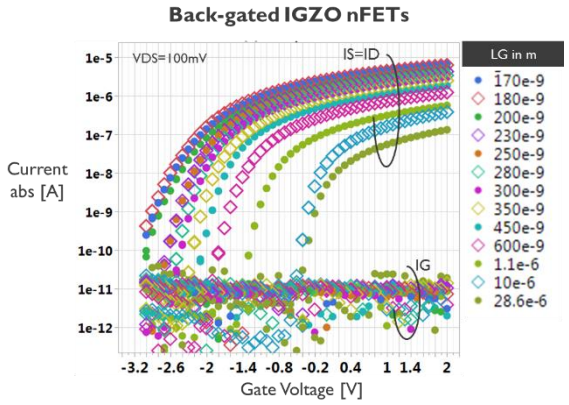

Fig. 4 I-V curves for a family of Back-gated IGZO nFETs

A clear modulation is seen, with a maximum measured I_{on}/I_{off} of approximately 7 decades. It must be noted that the I_{off} is at the floor of our inline measurement system. We also observe a negative V_{th} shift with reducing L_g, which is mainly related to controlling n-type H doping of IGZO, in addition to short channel effect. For better control of the channel, IGZO thickness can be scaled down, which is shown in Fig 5.

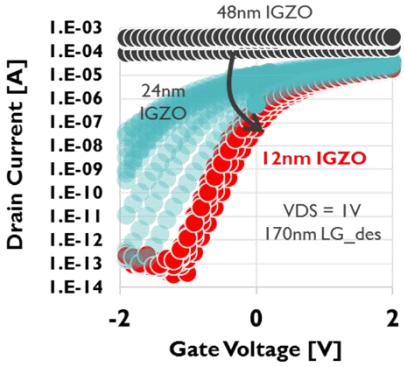

Fig. 5 Impact of a-IGZO thickness scaling on V_{th} swing

As mentioned, we assessed both a-IGZO and c-IGZO. Obtaining c-IGZO is achieved by tuning the O_2 ratio in Ar plasma during Pulsed DC PVD deposition, where O_2 ratios below certain limit "A" will result in a-IGZO formation, while ratios above that value will result in c-IGZO. We see that with c-IGZO the mobility values drop significantly and begin to approach a-IGZO only for increased O_2 ratios.

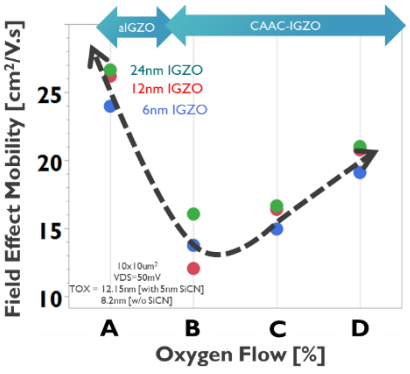

Fig. 6 Field effect mobility of a-IGZO and c-IGZO

In addition, we also see that although c-IGZO can give positive V_{th}, the latter has poorer electrostatic control compared to a-IGZO, and is more sensitive to thickness change, where c-IGZO thickness increase will result in a much more negative V_{th} swing as seen in Fig 7.

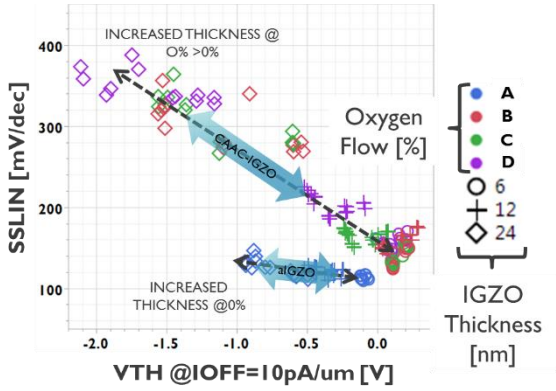

Fig 7. Electrostatics for a-IGZO and c-IGZO

Finally, we can compare our Back-gated IGZO nFETs to the reference Si device, which is shown in Fig 8.

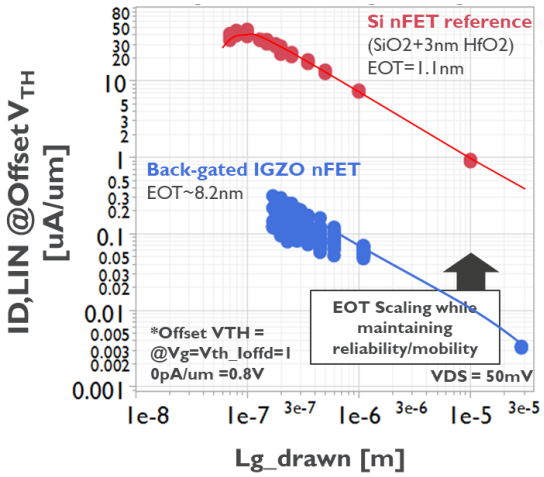

Fig. 8 Comparison of Back-gated IGZO nFETs with Si nFET reference

4. Conclusions

An integration scheme for enabling IGZO nFET fabrication in 300mm FAB has been demonstrated. Both a-IGZO and c-IGZO nFETs have been evaluated, with the data showing high mobility of 25cm^2/Vs, and better electrostatic control (110mV/dec) for devices utilizing a-IGZO. In addition, we see there is still significant room for IGZO device performance improvement by EOT scaling from current 8.2nm towards 1.1nm, which is used in reference Si nFET devices. This shows a high future potential for IGZO based nFET devices.

REFERENCES

[1] H. Kunitake et al., "High thermal tolerance of 25-nm c-axis aligned crystalline In-Ga-Zn oxide FET," IEDM, 2018.

[2] S. Wu et al., "Multi-Bit-per-Cell a-IGZO TFT Resistive-Switching Memory for System-on-Plastic Applications", IEDM, 2012.

[3] S. Yamazaki et al., "Properties of crystalline In–Ga–Zn-oxide semiconductor and its transistor characteristics," JJAP, 2014.