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Inverter Using CAAC-IGZO FET with 60-nm Gate Length Fabricated in BEOL

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Abstract

With use of FETs with a gate length of 60 nm including *c*-axis aligned crystalline (CAAC) indium-gallium-zinc oxide (IGZO) as an oxide semiconductor, an inverter composed of CAAC-IGZO FETs is prototyped and its operation is verified. A ring oscillator using the CAAC-IGZO FETs with controlled threshold voltages enables delay time with temperature changes to be suppressed, which suggests that the CAAC-IGZO FETs are suitable for constituting a logic circuit.

1. Introduction

Field-effect transistors using *c*-axis aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO FETs) have been widely adopted for LSI applications [1-6], as well as to displays. Utilizing the feature of extremely low off-state current of the CAAC-IGZO FETs [7], formation of memory for data backup in various circuits has been proposed to improve break even time (BET) necessary for power gating of the circuits [3, 8]. Since the channel of the CAAC-IGZO FET is formed on an insulator, it is possible to fabricate the CAAC-IGZO FET in a back end of line (BEOL) of a CMOS process [7]. With this advantage, a memory circuit with CAAC-IGZO FETs stacked over a CMOS circuit that is used to form peripheral circuits, has been reported [9]. The possibility of forming a simple logic circuit in the BEOL brings electrical selection of connection to the CMOS circuit.

This study shows characteristics of inverters using CAAC-IGZO FETs with a gate length of 60 nm (60-nm CAAC-IGZO FETs), especially such as temperature dependence of the delay time. Its measurement results validate a possibility of adopting our 60-nm CAAC-IGZO FETs to a logic circuit.

2. CAAC-IGZO FET

Figures 1 and 2 show a 60-nm CAAC-IGZO FET process flowchart and cross-sectional images of our prototyped CAAC-IGZO FET with a structure we call “trench gate self aligned (TGSA)” structure [7]. The gate length is 60 nm, the gate width is 60 nm, and the top gate insulator EOT is 6 nm. The In:Ga:Zn atomic ratio of the active layer is 4:2:3. CAAC-IGZO FET’s top gate electrode (TGE) and back gate electrode (BGE) are made of titanium nitride (TiN) and tungsten (W).

Figure 3 shows I_d-V_{gs} curves of the CAAC-IGZO FET at varied temperatures. Although the top gate insulator EOT is as large as 6 nm, the subthreshold swing at room temperature has a favorable value of 90 mV/dec. The drain current increases even when the temperature increases, which is opposite temperature dependence to Si FET [10]. Figure 4 shows the drain breakdown voltage and the gate breakdown voltage of the CAAC-IGZO FET, which shows that the CAAC-IGZO FET has a high breakdown voltage; specifically, the gate breakdown voltage is 3 V or higher and the drain breakdown voltage is 6 V or higher, in spite of the scaled gate length of 60 nm. Thus, the CAAC-IGZO FET can be an interface between a CMOS circuit and an external circuit.

3. Diode-connected Inverter using CAAC-IGZO FET

In this study, a diode-connected inverter [11] using CAAC-IGZO FETs was made. Figure 5(a) is a circuit diagram of the inverter that includes a transistor M1 and a transistor M2 as CAAC-IGZO FETs. Our prototype CAAC-IGZO FET is provided with a back gate electrode (BGE), at its lower part, with which the threshold voltage(V_{th}) is controlled dynamically. The BGE voltage (V_{bg}) of M2 in the inverter was varied, and DC performance was measured with varied V_{bg}. The actual measurement results are shown in Fig. 5(b), which verifies that V_{bg} as well as the FET dimension can control the logic threshold voltage.

We prototyped ring oscillators (RO) to evaluate dynamic performance of the inverters designed above. Figure 6(a) shows an RO circuit diagram, and Fig. 6(b) shows a die photo. We designed a 151-stage RO, to which an output buffer was connected to monitor the voltage waveform. The power supply voltage was set to 3.3 V. Figure 7 shows an output voltage waveform in one of cycle of the 151-stage RO, which exhibits an inverter delay of 142 ns.

Figure 8 shows temperature dependence of the delay time of the 151-stage RO, normalized at a room temperature. For comparison, Fig. 8 also shows delay-time evaluation results of an RO using a standard CMOS with a gate length of 60 nm (60-nm CMOS inverter) with SPICE simulation. The 60-nm CMOS inverter exhibited an increase in delay time by 14 % from the room temperature to 150°C. This change is derived from changes in V_{th} and mobility depending on temperatures. The RO using the 60-nm CAAC-IGZO FETs (60-nm CAAC-IGZO inverter) exhibited a decrease in delay time by 35 % from the room temperature to 150°C, which is derived from the CAAC-IGZO FET performance where the mobility increases even when the temperature increases. Moreover, the control of V_{bg} of the CAAC-IGZO FET reduces the amount of delay time change to 1 % or less. These results demonstrate

that the 60-nm CAAC-IGZO inverter enables the accelerated operation with an increase in temperatures and the constant operation with a simple correction circuit.

4. Conclusions

To verify the application of CAAC-IGZO FETs, inverters were made using 60-nm CAAC-IGZO FETs. Such inverters demonstrated reduction in performance variation depending on temperature changes. Applications of CAAC-IGZO FETs, to packaging technology due to their compatibility with BEOL process as well as to memory due to their ultra-low leakage current, are expected.

Fig.1. Process flowchart of 60-nm CAAC-IGZO FET.

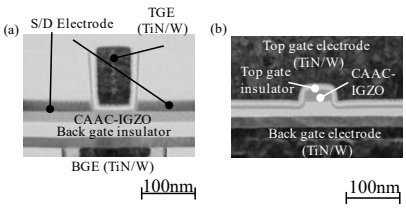

Fig. 2. Cross section of a 60-nm CAAC-IGZO FET in gate length direction (a) and in gate width direction (b).

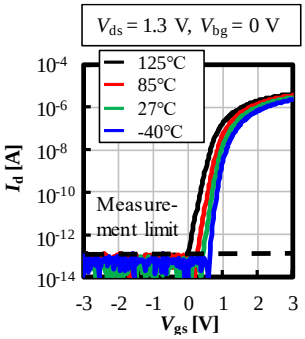

Fig. 3 Temperature dependence of I_d-V_{gs} curves of a 60-nm CAAC-IGZO FET.

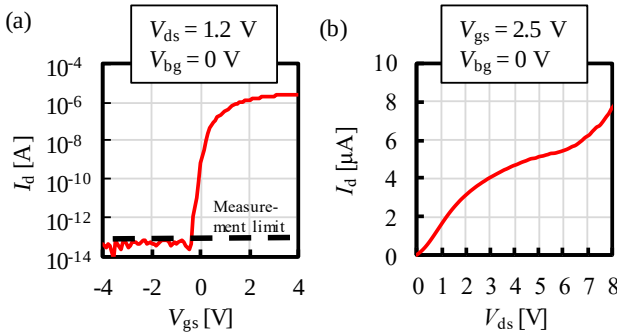

Fig. 4 Gate breakdown voltage (a) and drain breakdown voltage (b) of a 60-nm CAAC-IGZO FET.

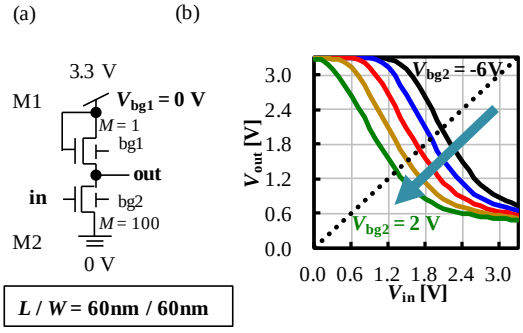

Fig. 5 Inverter circuit diagram using 60-nm CAAC-IGZO FETs (a) and DC analysis result (b).

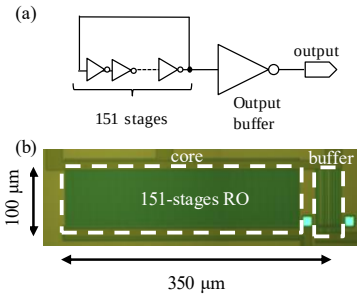

Fig. 6 Block diagram (a) and die photo (b) of 151-stage RO using 60-nm CAAC-IGZO FETs.

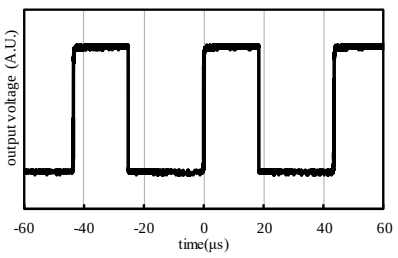

Fig. 7 An output voltage waveform of 151-stage RO.

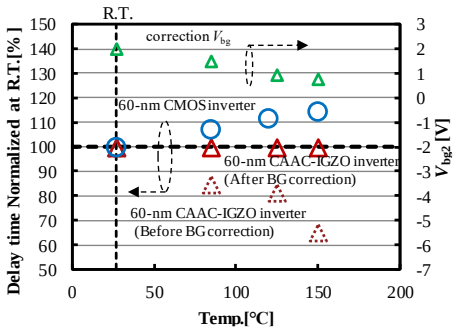

Fig. 8 Comparison of temperature dependence between ROs: 60-nm CAAC-IGZO FET inverters v.s. 60-nm CMOS inverters.

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