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Cost-Effective and BEOL-Compatible Double-Gate IGZO Recess-Channel TFT Technology Enables IoT ICs in More-than-Moore Era

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Abstract

We report BEOL-compatible, double-gated (DG) IGZO recess-channel TFT technology in film-profile engineering (FPE). A bi-layer organic photoresist (PR) floating-bridge was used as a shadow mask for the subsequent deposition of IGZO recess-channel and Al source/drain (S/D) electrodes on top of bottom-gate (BG) insulator of SiO_2 over p^+-Si (BG electrode). Following lift-off of the PR shadow mask as well as top-gate (TG) insulator deposition, a DG IGZO recess-channel TFT was fabricated with significant improvements in both I_{ON} and I_{OFF} in comparison to single-gated TFTs. Our proposed PR-FPE technique demonstrates the feasibility of IGZO recess-channel TFTs in various gated configurations, enabling a practically achievable building block for emerging applications in More-than-Moore Era.

1. Introduction

Integration of BEOL-compatible oxide-semiconductor (OS) TFTs with CMOS ICs promises cost-effective functionality and versatility for emerging IoT applications. While OS TFTs have been proposed for I/O bridging components [1], selection transistors in 3-D memory, [2] and IoT interface circuits [3], reports on boosting device performance and enriching device functionality in terms of gate-configuration designs, which have been extensively employed in advanced Si-CMOS multi-gate transistors, were few due to limited process tunability in OS materials. Our previous reports have proposed the practical realization of OS recess-channel TFTs in a novel "film profile engineering (FPE)" [4] scheme, in which a suspended hardmask bridge is deliberately constructed over the central region of active area in order for shadowing the subsequent deposition species for OS films and most importantly, for ingeniously tailoring the thickness of the OS channel that is thinner than that of S/D. High-performance OS TFTs [5] and 3-D inverters [6] have been demonstrated thanks to the OS recess-channels. However, the difficulty in removing the inorganic hardmask puts in limitations in the flexibility of device fabrication and the functionality of device operation. In this work we advanced our FPE technique with a bi-layer organic PR that can be easily removed afterwards for the fabrication of IGZO recess-channel TFTs with various gated structures as shown in Fig.1.

2. FPE Fabrication of IGZO multi-gated TFTs

Fig.2 illustrates the two-mask process flow for IGZO DG-TFTs fabrication. We started with a 50nm-thick CVD-SiO_2 (BG-insulator) deposition on a p^+-Si substrate (BG). A bi-layer PR of LOR/FH6400 was sequentially spin-coated and then subjected to lithographical exposure to delineate S/D fan-out (Fig. 2(a)). Under optimum development process conditions, a FH6400 floating-bridge was produced over a micro-cavity formed by underlying LOR (Fig.2(b)). Next FPE-films of IGZO and Al were sequentially deposited by RF sputtering and by thermal evaporation, respectively, with the nominal thicknesses of 40nm and 200nm. (Fig.2(c)). Detailed process conditions for these FPE layers are summarized in Table I. Removal of patterned PR completed the BG-TFTs fabrication (Fig.2(e)). Ford DG-TFTs, a bi-layer deposition of 30-nm-thick CVD-SiO_2 and 200-nm-thick Al was further made to serve as TG-insulator and TG-electrode (Fig.2(f)).

3. IGZO DG-TFTs

Formation of IGZO recess-channel structure is confirmed by AFM scanning (Fig.3). TEM observations (Fig.4) show the effectiveness of PR-FPE as evidenced by a gradual change in the thickness of IGZO film from the minimum thickness of 21nm in the channel (below the PR floating-bridge) to 44nm-thick in S/D. Another strong benefit gained from FPE is the formation of self-aligned Al electrodes on top of IGZO-S/D. The recess of IGZO channel as well as the selective deposition of Al electrode on S/D were practically realized by the optimum process conditions in terms of tailoring deposition pressure (P) during RF-sputtering (sufficiently high P) and thermal evaporation (ultra-low P). Fig.5(a) shows good switching behaviors of BG-TFTs with various channel length (L). The threshold voltage (V_{TH}) appears to increase with increasing L due to a reduction in channel thickness for long channels [4]. Fig.5(b) confirms good uniformity in device performance for IGZO TFTs that were fabricated by stable RF sputtering and evaporation processes. A DG-configuration for TFTs provides great flexibility for device operations in terms of applying bias voltages to BG and TG independently. Fig.6 compares transfer characteristics of IGZO TFTs in different operation modes in which external voltages applied to BG, TG, and both gates. For TG-mode, the TFT is driven by TG voltage with a floating BG, and vice versa for the BG-mode operation. Steeper SS and a large increase in I_{on} are simultaneously achievable for IGZO TFTs in DG mode when both BG and TG are tied together and biased at the same voltage. Output characteristics of TFTs shown in Fig.7 clearly exemplifies that current drivability could be dramatically enhanced by gate-configuration design from BG through TG to DG. It is clearly seen in Fig.7(c) that the sum of drive currents measured in TG- and BG modes are much lower than that of TFTs in DG mode, which is attributable to effective modulation of the channel potential by the strong coupling of these two gates [7]. Fig.8 further shows that V_{TH} can be effectively modulated for TFTs operating in TG mode in combination with BG as an auxiliary gate. Fig.9 depicts envisioned features by implementing our proposed FPE TFTs to BEOL of a CMOS chip. Note that, while the OS recess-channel is prepared by sputtering, S/D metal can be deposited by using ionized metal plasma (IMP) tools with depositing species of highly unified directionality. The BG TFTs can be placed in the outmost layer with one side of the OS channel exposed for environmental gaseous or bio sensing. Meanwhile, DG and complementary OS TFTs can be embedded within the multi-level interconnects for numerous functional circuit applications. With some process modifications, the TG of the OS devices can be patterned in a damascene step simultaneously on the same level of interconnect.

4. Conclusion

We demonstrated a novel BEOL-compatible IGZO recess-channel TFT technology that can be readily applied in

practical manufacturing. In our proposed scheme a disposable PR suspended bridge is formed to shadow subsequent deposited films with tailorable profiles in thickness. Both BG and DG configuration can be realized in this approach which greatly increase the functionality of device operations. Moreover, DG-mode operations also effectively boost the device performance and augment the operation flexibility.

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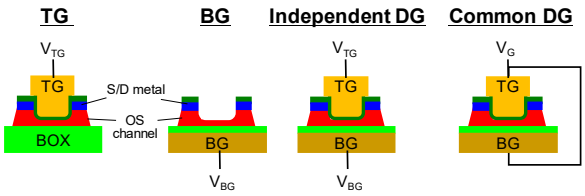

Fig.1 Various gated configurations are feasible with the BEOL TFTs.

TABLE I. Key Process Parameters of FPE Steps.

	Instrument	Temp.	Pressure	MFP	Profile Feature
Channel (IGZO)	RF Sputter	R.T.	5 mTorr	~1 cm	Recess-channel
S/D Metal (Al)	Thermal Coater	R.T.	8x10^{-6} Torr	~5 m	Discrete S/D metal

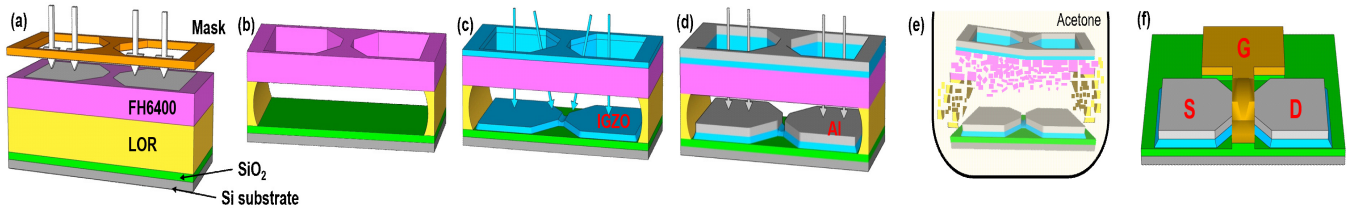

Fig.2 Process flow of IGZO recess-channel TFT: (a) Lithographical patterning of bi-layer PR (FH6400/LOR) to define S/D fan-out regions. (b) Formation of a FH6400 bridge suspending over a LOR micro cavity, followed by sequential depositions of (c) IGZO channel and (d) Al S/D pads. (e) PR Lift-off. (f) Formation of top-gate oxide and top gate electrode.

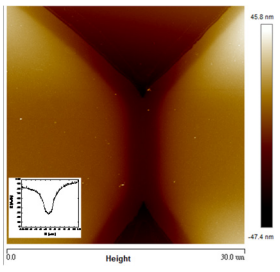

Fig. 3 AFM scan mapping of a test sample after the IGZO deposition and PR lift-off.

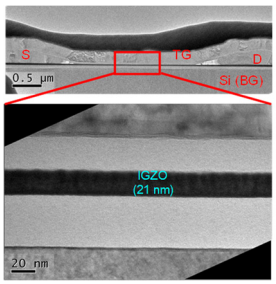

Fig. 4 Cross-sectional TEM image of a fabricated DG-TFT. The IGZO channel thickness is 21 nm.

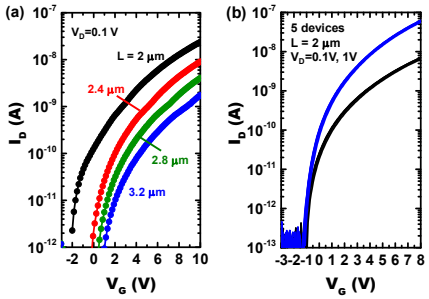

Fig. 5 Transfer characteristics of (a) BG-TFTs with L ranging from 2 to 3.2 μm and (b) five BG-TFTs (L = 2 μm) located at different dies within a 4" wafer.

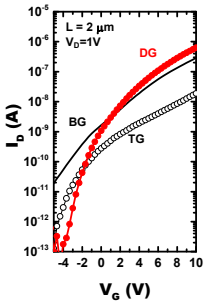

Fig. 6 Transfer characteristics of a DG-TFT operating at TG, BG, and DG modes respectively.

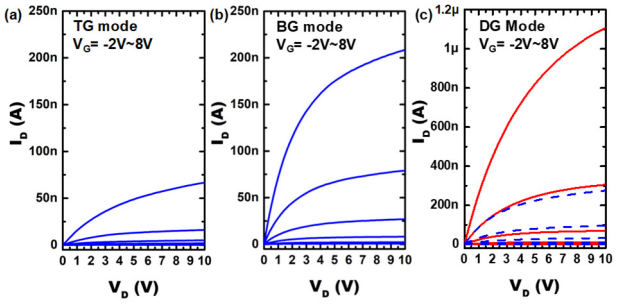

Fig. 7 Output characteristics of a DG-TFT operating at (a) TG, (b) BG and (c) DG modes, respectively. In (c) the sum of drain currents from TG and BG modes is also shown (dashed lines) for comparison.

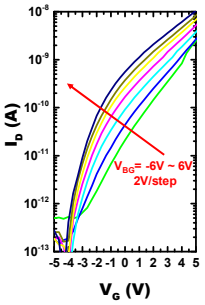

Fig. 8 Transfer curves of a DG-TFT driven by TG in combination with an auxiliary BG bias ranging from – 6 to 6 V.

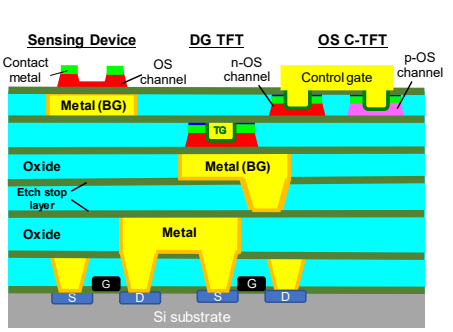

Fig. 9 Envisioned schemes for implementing OS TFTs of various gated configurations to BEOL of an CMOS IC chip.