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Grain Growth Control with a Dot Mask in Selective Laser Annealing for Stable LTPS Thin Films Transistors Fabrication

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Abstract

We propose an effective method for selective laser annealing of low-temperature poly-Si thin films in response to the demands of flat panel display manufacturing. Si thin film transistors with high mobility and stable characteristics were successfully obtained by controlling the grain boundaries of Si films with a dot mask and reduction projection lens.

1. Introduction

Low-temperature poly-Si (LTPS) thin film is one of the promising channel materials for Si thin film transistors (TFTs). It exhibits higher mobility than amorphous Si (a-Si) and has the potential to be applied in both organic light-emitting diodes (OLEDs) and liquid active-matrix liquid crystal displays (AMLCDs).

An essential process for LTPS fabrication is excimer laser annealing (ELA) using KrF or XeCl excimer lasers, which enable the crystallization of Si thin films with high performance and throughput. In particular, line-beam delivery systems scanning in the short-axis direction with multiple excimer laser sources are used commercially for small or medium substrates. Recently, a selective laser annealing (SLA) technique has been developed to respond to the demands of large-scale panel mass production such as G10.5[1]. However, one remaining issue with this process is the difficulty of obtaining uniform TFT characteristics due to the random grain size and location.

In this study, we propose a method for fabricating high-stable TFTs with a KrF excimer laser. The location, size, and shape of poly-Si grains can be controlled precisely via a dot array mask and reduction projection lens without scanning exposure. In this process, a short wavelength of the KrF excimer laser (248 nm) is suitable owing to its high resolution. A lateral solidification phenomenon is induced by unmelted seeds generated between high and low temperature Si. Several techniques have been proposed, such as sequential lateral solidification (SLS)[2] and phase modulated excimer laser annealing (PMELA)[3], for producing location-controlled single-crystal regions. Our approach is to improve the uniformity of poly-Si grain boundaries to fabricate stable TFTs. We report the characteristics of LTPS TFTs fabricated by SLA with a dot mask.

2. Experimental Methods

A schematic of the experimental setup is shown in Fig. 1. We used a KrF excimer laser (Gigaphoton. Inc, wavelength: 248 nm, pulse duration: ～30 ns) with a beam spot of 150 μm × 150 μm on the substrate. In SLA, the microlens array (MLA) is located at the pixel pitch, and can produce multiple beams to apply SLA only to the TFT region. In addition, an optical delay system that can stretch the pulse width of the laser was installed to enhance the flexibility of grain sizes. An infinity-corrected objective lens (× 20) and a dot mask (square-shaped array) of Al films (~ 100 nm) on a quartz substrate were used in this setup to create contrast between the beam profile and the uniform square-shaped grains of poly-Si by inducing lateral growth. First, a-Si (100 nm) films were deposited onto the quartz substrate by low-pressure chemical vapor deposition (CVD) at 550 °C. Then, SLA was conducted at fluence range of 700–1000 mJ/cm^2 and shot count of 10 shots.

After laser irradiation and polycrystallization, the top gate transistors (Fig. 2) were fabricated as follows. The Si film was patterned by photolithography and wet etched with a mixture of HF, HNO_3, and H_2O. For the gate insulator, SiO_2 film (100 nm) was deposited, and TiN (150 nm) electrode film was deposited and patterned.

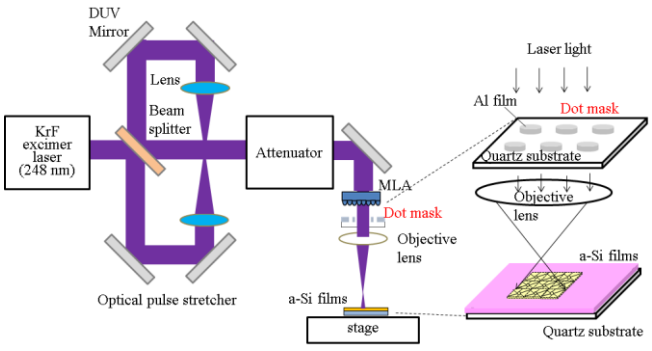

Fig. 1 Schematic of the laser annealing system with a dot array mask and reduction projection lens.

Ion implantation of As^+ 140 keV with a dose of 5×10^{15} cm^{-2} was carried out to form the source/drain, followed by the annealing activation in the N_2 ambience at 550 ºC for 6 h. Then, the dielectric film of SiO_2 (~200 nm) was deposited by atmospheric pressure CVD at 400 ºC. The contact holes were opened by wet etching, and the contact metal of Al films were deposited and patterned. Finally, H_2 sintering was performed at 400 ºC for 0.5 h.

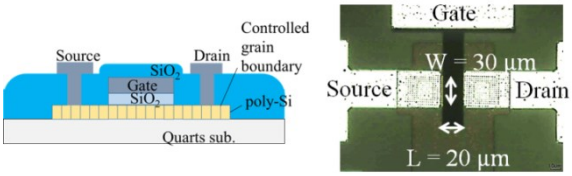

Fig. 2 Cross-section image (left) and optical micrograph (right) of the top gate TFT.

3. Results

Fig. 3 shows the scanning electron microscope (SEM) images of Si films annealed with a dot mask. Homogenously square-shaped boundaries of ~1.5 μm on one side and periodic protrusions were confirmed under the condition of 900 mJ/cm^2 and 10 shots. Lateral growth phenomenon was clearly observed at high laser-fluence, inducing near complete melting of the Si. It was assumed that lateral grain growth occurred from the solid a-Si in the shadow region formed via a dot mask to the round liquid Si region irradiated by the laser light. Therefore, it is possible to control the grain sizes and locations of Si films by creating high contrast between beam profiles with a dot mask.

In Fig.4, the histograms of grain sizes (N=20) annealed by the conventional ELA without mask (Fig. 4 (a)) and SLA with a dot mask (Fig. 4 (b)) are shown. The sigma of grain size significantly decreased from 27 % to 3.9 % for the SLA with a dot mask.

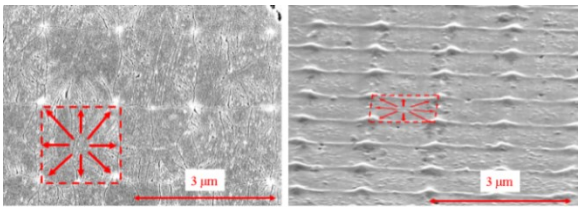

Fig. 3 SEM images of Si films (left: secco-etched Si surface and tilt = 0°; right: no secco-etched Si surface and tilt = 70°) at fluence of 900 mJ/cm^2 and 10 shots.

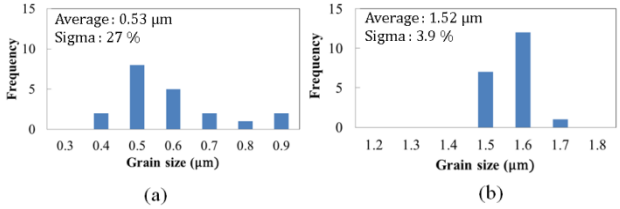

Fig. 4 Histgrams of grain sizes, (a) conventional ELA without mask at fluence of 700 mJ/cm^2 and 20 shots, (b) SLA with a dot mask at fluence of 900 mJ/cm^2 and 10 shots.

Fig. 5 shows the transfer curves (drain current (I_D)−gate voltage (V_G) characteristics) of the top gate TFTs fabricated by SLA with the square-shaped dot mask at drain voltage (V_D) = 0.05 V for fluences ranging from 700 to 1000 mJ/cm^2 and 10 shots. As shown in Fig. 5, high field effect mobility (μ_{FE}) of over 60 cm^2/Vs was confirmed at all fluences. It is thought that grains of ~1.5 μm were formed laterally at overall regions because the energy density was sufficient to induce complete melting of irradiated Si, while the shadow regions of Si were prevented from being fully melted. In addition, low leak current of ~pA and high on/off ratio of over ~10^6 were obtained. It is known that the characteristics of LTPS TFTs fabricated by conventional ELA greatly depend on the laser fluence; thus, severe control of fluence is required. On the other hand, grain-controlled LTPS TFTs with a dot mask showed relatively stable characteristics regardless of the laser fluence. As a result, the sigma of the μ_{FE} of LTPS TFTs (N=8) for SLA with a dot mask at the fluence of 900 mJ/cm^2 and 10 shots drastically decreased from the conventional ELA of 17 % to 2.8 %.

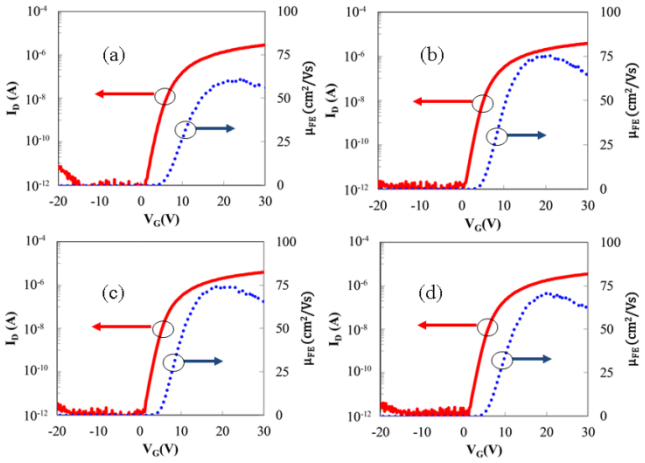

Fig. 5 Transfer curves of the top gate TFTs at the drain voltage (V_D) = 0.05 V at the fluences of (a) 700 mJ/cm^2, (b) 800 mJ/cm^2, (c) 900 mJ/cm^2, (d) 1000 mJ/cm^2 and 10 shots.

4. Conclusions

The proposed grain growth control technique with a dot mask was shown to be useful and applicable in fabricating LTPS TFTs in large-scale flat panel displays.

Acknowledgements

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