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Impact of As Doping in Amorphous Ge on Solid-Phase Crystallization

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Abstract

As doping in amorphous Ge significantly promoted the lateral growth during solid-phase crystallization, resulting in large grains (19 μm). The electron mobility (370 cm^2/Vs) was the highest among n-type polycrystalline Ge directly grown on insulators at low temperatures (< 900 °C).

1. Introduction

Low-temperature synthesis of polycrystalline (poly-) Ge on insulators is a key technology to integrate Ge-CMOS into existing devices. We recently fabricated a poly-Ge layer with a hole mobility of 620 cm^2/Vs by using solid phase crystallization (SPC) of a densified amorphous (a-) Ge at 500 °C [1]. However, n-type poly-Ge on insulators with high electron mobility (> 200 cm^2/Vs) have yet to be achieved. In present study, we aimed at the fabrication of n-type poly-Ge with high electron mobility using SPC with As doping.

2. Experimental Procedures

As-doped Ge precursors (200 nm thickness) were deposited on SiO_2 glass substrates at RT using a Knudsen cell of a molecular beam deposition system. To modulate the As concentration of the Ge layer, the temperature of the As Knudsen cell, T_{As}, ranged from 200 to 270 °C. Using secondary ion mass spectrometry (SIMS), the As concentration was determined to be 2.8×10^{19} cm^{-3} for T_{As} = 210 °C, 1.2×10^{20} cm^{-3} for T_{As} = 230 °C, and 5.9×10^{20} cm^{-3} for T_{As} = 250 °C, which were constant regardless of before and after annealing. The samples were then loaded into a conventional tube furnace under a N_2 (99.9%) atmosphere and annealed at a growth temperature, T_g, of 450 °C for 5 h and 375 °C for 140 h to induce crystallization. For all samples, we performed post annealing (PA) at 500 °C for 5 h. The grown layers were analyzed by the Raman measurement, electron backscattering diffraction (EBSD) measurement, and Hall effect measurement (van der Pauw method).

3. Results and Discussion

Fig. 1(a) shows that the samples with T_g = 450 °C exhibit sharp peaks near 300 cm^{-1}, corresponding to crystalline (c-) Ge-Ge bonding in the whole T_{As} range. These peaks are almost symmetrical, suggesting that the Ge layers are completely crystallized. As representatively shown in Fig. 1(b), annealing at 375 °C for 140 h crystallized the samples with $T_{As} \leq 240$ °C, but not those with $T_{As} \geq 250$ °C. This is likely because segregation of excess As suppressed nucleation. The Raman shift and the full width at half maximum (FWHM) of c-Ge peaks were evaluated from the Raman spectra and are

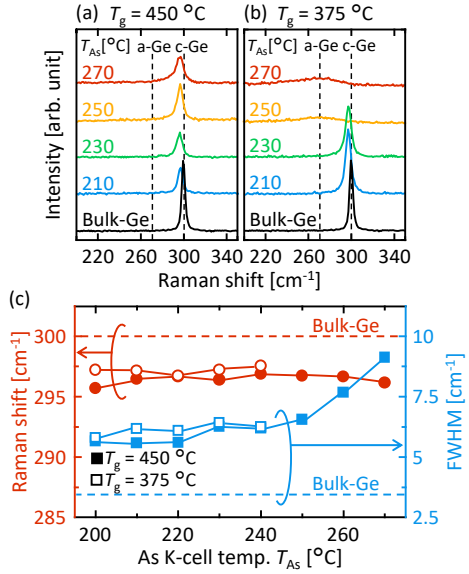

Fig. 1. (a,b) Raman spectra of the samples with T_g = (a) 450 and (b) 375 °C. (c) Raman shift and FWHM of the Ge-Ge peaks as a function of T_{As}.

summarized in Fig. 1(c). All peaks shifted to lower wavenumbers than that of a bulk Ge substrate, originating from the tensile strain. The peak shifts are almost constant with respect to T_{As} while the peaks for T_g = 450 °C shifted to the lower wavenumber than that for T_g = 375 °C. This behavior suggests that the strain likely originates from the difference in the thermal expansion coefficients between Ge and the SiO_2 substrate. FWHM is almost constant for $T_{As} \leq 240$°C and significantly increases with T_{As} for $T_{As} \geq 250$°C.

Fig. 2(a)–2(d) shows that the grain size dramatically varies with T_{As}. Fig. 2(e) shows that the average grain size increases with increasing T_{As} and then begins to decrease. The decrease in grain size at higher T_{As} (≥ 250 °C) is likely attributed to the suppression of lateral growth caused by segregation of excessive As. This behavior well accounts for the results of the Raman FWHM. In contrast, when doping amount of As is sufficiently small ($T_{As} \leq 240$ °C), the grain size increases with T_{As}, suggesting that As atoms accelerated the lateral growth of Ge. A similar behavior has also been reported in Sn and Sb doped SPC-Ge [2,3]. The lower T_g provides a larger grain size, which agrees with the non-doped SPC-Ge [1]. The sample with T_{As} = 230 °C and T_g = 375 °C exhibited a grain size of 19 μm, which is the largest among poly-Ge formed by SPC.

The electrical properties were evaluated and shown in Fig. 3. All samples showed n-type conduction owing to the self-organizing activation of As during SPC. We first discuss

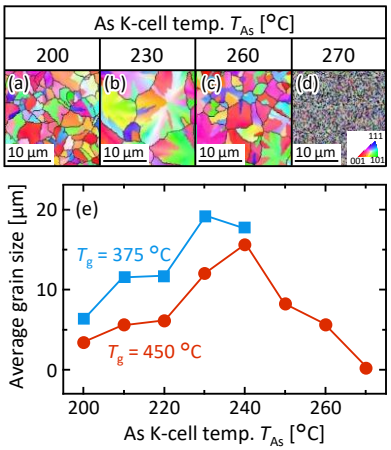

Fig. 2. (a-d) EBSD images of the samples with T_g = 450 °C and T_{As} = (a) 200, (b) 230, (c) 260, and (d) 270 °C. (e) Average grain size as a function of T_{As} for samples with T_g = 375 and 450 °C.

the data before PA. Fig. 3(a) shows that electron concentration n for T_g = 375 °C is lower than that for T_g = 450 °C in the whole T_{As} range. This is attributed to the fact that lower T_g has the lower solid solubility of As in Ge. Fig. 3(b) shows that electron mobility μ_n tends to increase with increasing grain size. However, for T_{As} = 230 °C, μ_n for T_g = 375 °C are lower than those for T_g = 450 °C, which may reflect larger carrier scattering caused by more segregation of excess As. PA improved the electrical properties of the samples. Fig. 3(a) shows that n for T_g = 450 and 375 °C increases to the similar value by PA for each T_{As}. n is maximized at around T_{As} = 230 °C where the grain size is maximum (Fig. 2(e)). This behavior is likely because the larger grain size provides the lower defect-induced acceptors and/or the less As segre gation at grain boundaries. Fig. 3(b) shows that μ_n increases by PA in whole T_{As} range, reflecting the decrease of carrier scattering by inactive As.

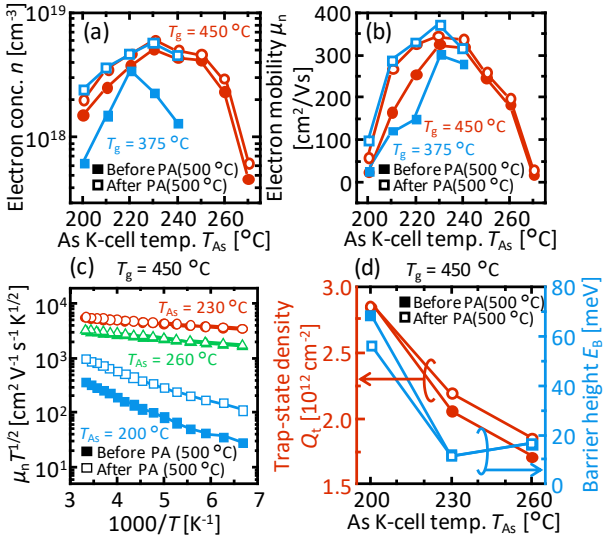

Fig. 3. (a,b) Electrical properties of the samples with T_g = 375 and 450 °C before and after PA (500 °C) as a function of T_{As}. (c) Arrhenius plot of $\mu_n T^{1/2}$ for samples with T_{As} = 200, 230, and 260 °C. (d) Trap-state density Q_t and energy barrier height E_B as a function of T_{As}.

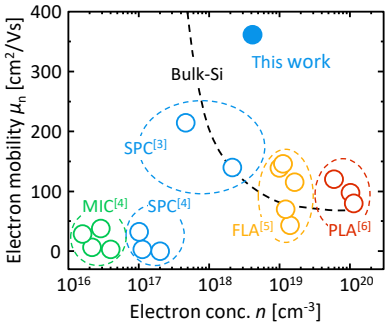

Fig. 4. Comparison of the electron mobility μ_n and electron concentration n of poly-Ge on insulators.

According to the carrier conduction model proposed by Seto for polycrystalline semiconductors, μ_n limited by grain-boundary scattering can be determined by using the following equation:

$$\mu_n T^{1/2} = \frac{Lq}{\sqrt{2\pi m^* k}} \exp\left(-\frac{E_B}{kT}\right)$$

where E_B is the energy barrier of the grain-boundary, T is the absolute temperature, L is the grain size, q is the elementary charge, m^* is the effective mass, and k is the Boltzmann constant. Fig. 3(c) shows that the Arrhenius plot of $\mu_n T^{1/2}$ makes almost-downward-sloping straight lines for whole T_{As} region. The trap-state density Q_t in the grain boundaries can be determined by using the following equation:

$$Q_t = \frac{\sqrt{8\varepsilon n E_B}}{q}$$

where ε is the dielectric permittivity. Fig. 3(d) shows that Q_t decreases with increasing T_{As}, suggesting that As atoms passivate the grain boundary traps. The minimum value of E_B is obtained for the highest μ_n sample with T_{As} = 230 °C.

As shown in Fig. 4, the μ_n of 370 cm^2/Vs obtained in this study is the highest value among the Ge layers formed on insulating substrates at temperatures below the melting point of Ge (937 °C). The findings in this study will provide a pathway for the monolithic integration of high-performance Ge- CMOS ont o Si-LSIs and flat-panel displays.

4. Conclusions

As doping into an a-Ge precursor significantly influenced the subsequent SPC. By optimizing As amount (T_{As} = 230 °C) and lowering T_g (375 °C), the grain size reached 19 μm. The subsequent PA (500 °C) provided the highest electron mobility (370 cm^2/Vs) among n-type poly-Ge directly grown on a glass substrate.

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