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High mobility Si TFTs on crystalline Si stripe formed by micro chevron laser beam scanning

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Abstract

Top gate n-ch thin film transistors (TFTs) were fabricated on crystalline Si stripe having grain length more than hundred microns that was formed by micro chevron laser beam scanning method. Here sputtering SiO_2 was used as gate insulator of TFTs. Maximum field effect mobility was 422cm^2/Vs, with subthreshold swing of 0.485 V/Dec and on/off ratio of 2.8 x 10^6.

1. Introduction

Resolution as well as definition have been increasing in flat panel displays with all sizes since its advent in market several decades before. For small size OLED displays, increasing definition result in miniaturization of pixel size and pixel driving TFTs. Variations in the number of grain boundaries within the channel of pixel driving poly-Si TFTs come to the surface, which cause luminance unevenness among pixels. For large size LCD displays, increasing resolution and flame rate will shorten selected term of a gate line, so higher mobility is demanded. In order to match the above demands for all display sizes, we have proposed micro-chevron laser beam scanning (μCLBS) method[1] for forming long grain crystalline Si stripe. In this method, μCLB, was formed by passing an output of multi-mode UV laser diode through a one-sided Dove prism (Fig.1), and was scanned through Si film to form 5-7 μm wide crystalline Si stripe having grain length more than hundred microns at the scanned path. In recent by adding SiO_2 capping film with a thickness more than 200 nm on the Si film, (100)-faced single grain with a length more than 3mm was also formed. In this study, TFTs was fabricated on the crystalline Si stripe without using SiO_2 capping film on Si, and characteristics of the TFTs will be shown.

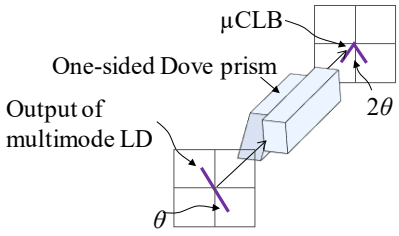

Fig.1 Mechanism of μCLB formation

2. Experimental method

Figure 2 shows fabrication process of TFTs. 1. Dehydrogenated 60nm-thick CVD a-Si film on SiO_2 film as precursor for laser crystallization. 2. About 10μm-wide crystalline Si stripe was formed in Si film by μCLBS, and then non annealed amorphous Si region was selectively removed by a-Si etchant to leave only the crystalline Si stripe as channel island of TFTs without using photolithography technique. Figure 3 shows schematic of μCLBS system here. 3. 100nm-thick SiO_2 film was deposited on the Si stripe by reactive pulse DC sputtering method at 340°C as a gate insulator. 4. 300nm-thick Al gate electrode was formed by sputtering through the 1st metal mask. 5. S/D ion implantation at an acceleration voltage of 80 keV and at a dose of 3 x 10^{13}cm^2. 6. Capsulation of channel region by 200nm-thick sputtering SiO_2 film through the 2nd metal mask at room temperature. 7. S/D region dopant activation at 550°C in vacuum for 0.5h. 8. SiO_2 film on S/D region removed by 1% HF solution to expose S/D region for contact. 8. S/D Al electrode deposition using sputtering through 3rd metal mask 9. Forming gas (~5% H_2 in N_2) annealing (FGA) at 400°C and at 1atm for 0.5 h as a 1st post

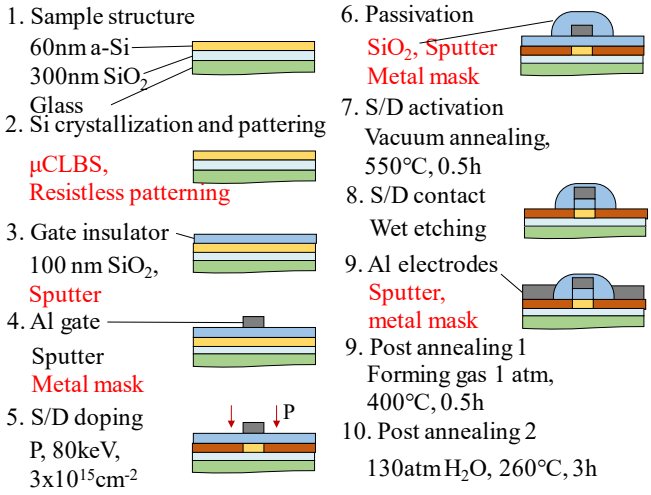

Fig. 2 Fabrication process of TFTs

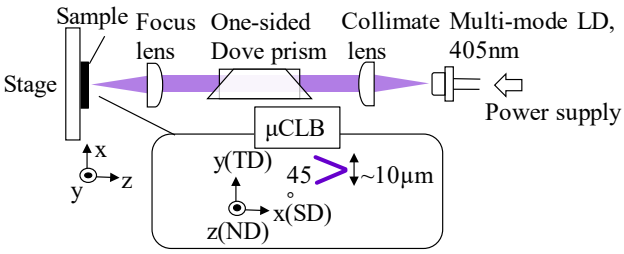

Fig. 3. Schematic figure of μCLBS system

annealing. 10. 120 atm high pressure H_2O annealing (HPA) at 260ºC for 3h for the 2nd post annealing. Effect of two general post annealing method on TFT characteristics was compared.

3. Results and discussion

Figure 4 shows scanning electron microscopy (SEM) image of crystalline Si stripe with a tilting angle of 70º. The laser scanning direction is from downside toward upside in the figure. The stripe is convexed and smooth at the center which was a single lateral grain, and is flat and longitudinally undulated toward outside at the side region which was composed of longitudinal lateral grains. The stripe is thick at the center because of agglomeration during melting, and is very flat at that region because no impingement of lateral growth grain there.

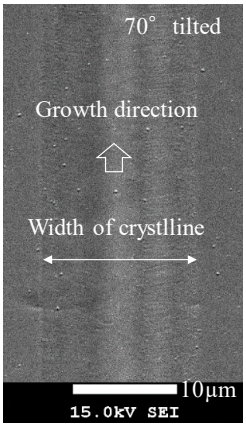

Fig.4 SEM image of Si stripe

Figure 5 shows optical microscope image of fabricated TFTs. TFT channel region was formed on crystalline Si stripe.

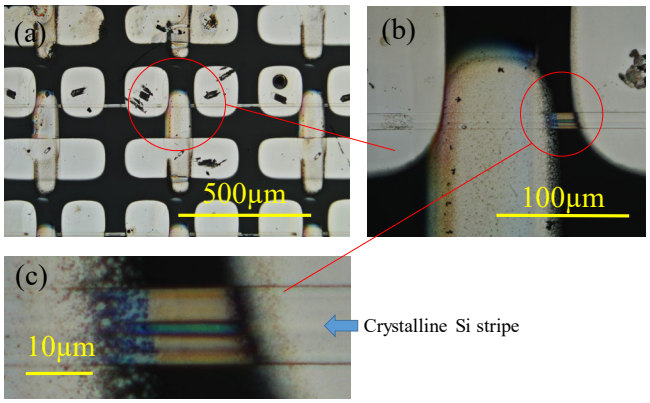

Fig.5 Optical micrograph of fabricated TFTs

Blue colored region at the center of crystalline Si stripe in Fig.5(c) again indicates a thicker film thickness there. The channel dimension was measured from Fig.5 to be L/W=95.2µm/11.2µm.

Figure 6(a) and Fig.6(b) shows respectively I_dV_g and I_dV_d characteristics. In Fig.6(a), both gate leak current I_g (V_d =0.1V) and electron field effect mobility μ_n were also shown. The μ_n were calculated from transconductance of the TFT at V_d of 1V, and have been confirmed to be the same as a value calculated at V_d of 0.1V. Parameter of the TFT were summarized in Table.1. The maximum μ_n was 422 cm^2/Vs, thanks to single grain Si stripe formed by µCLBS. This value is expected to be further increased if lateral grains at the side region of crystalline Si stripe can be removed. Besides, it is worth noting that sputtering SiO2 film was used as gate insulator here. S value might be lower than that in TFTs with CVD SiO_2 due to surface high energy particle impingement during sputtering, but this value is still acceptable for actual

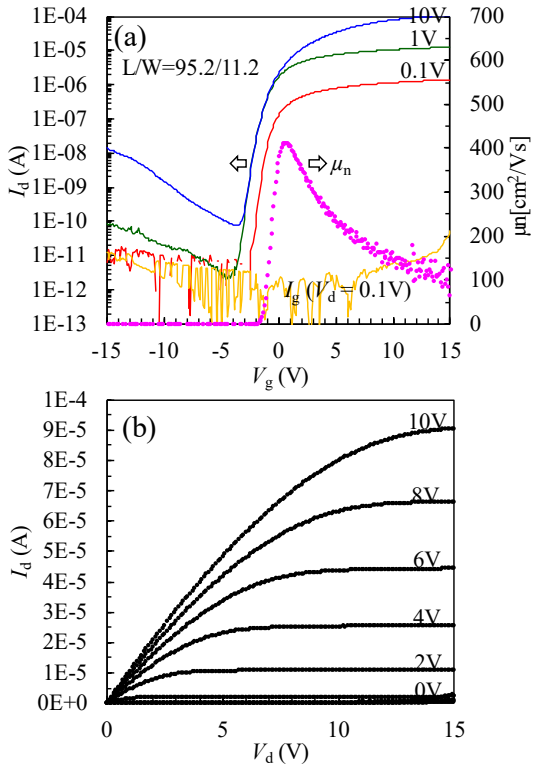

Fig.6 IV characteristics of a TFT

Table.1 Parameters of the TFT

μ_n	422 cm^2/Vs (Maximum value)
V_{th}	-1.4 V
S	0.485 V/dec. (Average value)
$R_{on/off}$	2.8 × 10^6 (Id@Vg =5V to -5V)

application to displays. Besides, there is no significant difference on characteristics between TFTs after FGA and further after HPA.

4. Conclusions

Top gate n-ch TFTs were fabricated on crystalline Si stripe having grain length more than hundred microns that was formed by micro chevron laser beam scanning method. Here sputtering SiO_2 was used as gate insulator. Maximum field effect mobility was 422cm^2/Vs, with subthreshold swing of 0.485 V/Dec and on/off ratio of 2.8 x 10^6. The µCLBS method is expected to provide a new method for fabricating high mobility TFTs.

Acknowledgements

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References

[1] W. Yeh, S. Yamazaki, A. Ishimoto and S. Morito, APEX 9,025503(2015).

[2] W. Yeh, T. Shirakawa, A.H. Pham, and S. Morito, Jpn. J. Appl. Phys., 58, SBBJ06 (2019).