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Low Temperature Poly-Si Junctionless TFTs with Low Temperature Cyclic Trimming Process for 3D-ICs and Low Power Applications

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Abstract

Low temperature trimming process is developed to stably scale the junctionless device within nanoscale without surface degradation for low standby power applications. On/Off-current ratio and I_{off} reaches $5x10^7$ and $1x10^{-15}$ (A/μm) with 3 nm channel thickness. Electrical performance is compared. Interestingly, subthreshold swing shows degradation which gives us an insight into the vertical crystallinity profile within few nanometers.

1. Introduction

Recently, low temperature polycrystalline silicon (poly-Si) and junctionless (JL) devices are vastly studied due to its great potential in monolithic 3D-ICs (M3D-ICs), and system-on-panel (SOP) applications to expand the more-than-Moore (MtM) plateau [1]. The idea is to directly fabricate JL device on an insulation layer within low temperature which meets the criteria of low thermal budget and good CMOS compatibility [2, 3]. The absence of p/n junction makes JL device insensitive to thermal process; its depletion operation makes it meets the reliability standard for M3D-ICs [4]. At the same time, power consumption is also a major concern for nowadays electronics, in that sense, considering the heavily doped channel of JL devices, in order to effectively turn off the device and to further suppress the off-state current (I_{off}), a cyclic low-temperature trimming process was developed to well control the channel dimension in nanometer scale. An ultra-thin body (UTB) with rather large channel dimension is used in this work to rule out the other structural impact on the device performance and to authentically reflect the electrostatic changes with each trimming cycles.

2. Device Fabrication

A sequence of major processes are listed in Fig.1 (a). 6 inch wafer is used. After wet-oxide was grown to simulate the interlayer dielectric (ILD) of the first layer device, 100 nm phosphorus in-situ doped poly-Si (DP) was deposited and etched into raised-source/drain (R-S/D) [Fig.1 (b)]. Subsequently, a 10 nm thin DP was deposited as channel connecting S/D. After standard solid phase crystallization (SPC) to crystallize and activate the dopant, active area (AA) was patterned with mesa isolation [Fig.1 (c)]. The cyclic low-temperature trimming process was performed at this stage as described as follow. A layer of chemical oxide was grown by H_2O_2 (31%) solution under 75 °C with 10 min [Fig.1 (d)], followed by selective etch of the grown chemical oxide via diluted HF (DHF) as a completion of a cycle [Fig.1 (e)]. The average etch rate (E/R) of the process is around 1 nm/cyc. After numerous trimming cycles, channel thickness was monitored by ellipsometry and etched till 5/4/3 nm respectively. Then, another layer of chemical oxide was grown with the same condition as interfacial layer (IL), followed by atomic layer deposition (ALD)-AlO_x/HfO_x, post deposition anneal (PDA), ALD-TiN, and physical vapor deposition (PVD)-TiN as gate stack. After gate patterning by dry etch, 100 nm of plasma-enhanced chemical vapor deposition (PE-CVD) TEOS oxide spacer was formed to finish the device [Fig.1 (f)]. Fig.1 (g) shows the top view of the planar device.

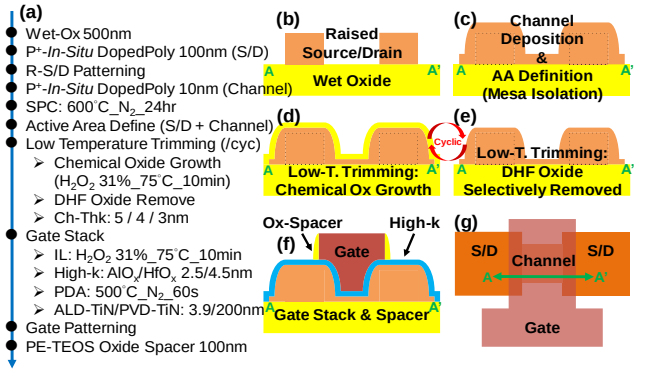

Fig.1 (a) List of major fabrication process. (b) R-S/D deposition and patterning. (c) DP channel deposition and AA definition. Cyclic trimming process is described as a combination of (d) chemical oxide growth and (e) selective etch of the grown oxide by DHF. (f) Device final structure with gate stack and gate spacer. (g) Top view of the planar device with green arrow marking the cross-section where (b-f) is showing.

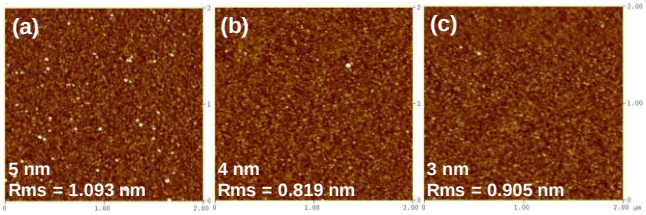

Fig.2 AFM surface roughness analysis with T_{Si} (a) 5 nm, (b) 4 nm, and (c) 3 nm. No surface morphology degradation is observed which is critical to nanoscale devices.

3. Result and Discussion

Choose of Chemical Oxide

The idea of using chemical oxide for trimming process came from the IL growth. The grown chemical oxide thickness of different immersion time of the sample (not shown) shows that it saturates after 400 s as well as the trimmed thickness of the DP channel. The self-limit property is appealing to nanofabrication. Also, during the cyclic trimming process, we monitored the thickness (T_{Si}) change of each cycles, the E/R are all around 1 nm/cyc. while using SC-1 solution

($NaOH:H_2O_2:H_2O$ = 1:4:20, 75 °C), the E/R accelerates, making it hard to control the thickness less than 6 nm. Another advantage of the process is that the surface roughness shows no degradation by the AFM analysis in Fig.2 which is a crucial factor for nanoscale device.

Electrical Performance in T_{Si} = 5/4/3 nm

Transfer and output characteristics of T_{Si} = 5/4/3 nm are compared with device dimension and equivalent oxide thickness (EOT) listed in Fig.3. It is obvious that the threshold voltage (V_{th}) shifted positively [Fig.3 (a)], and I_{off} is significantly suppressed. A collective comparison of various parameters are shown in Fig.3 (b-d). V_{th} in Fig.3 (b) shows 2.5 V shift from 5 to 3 nm which suggest that the channel doping is very high. As T_{Si} is scaled, there will be less surface potential needed to fully deplete the highly doped channel. Drain-induced-barrier-lowering (DIBL) in Fig.3 (c) is rather small with no obvious difference. Interestingly, subthreshold swing (S.S.) shows degradation with T_{Si} scaling [Fig.3 (d)]. S.S. can reflect both interface quality and channel crystallinity which will be discussed later.

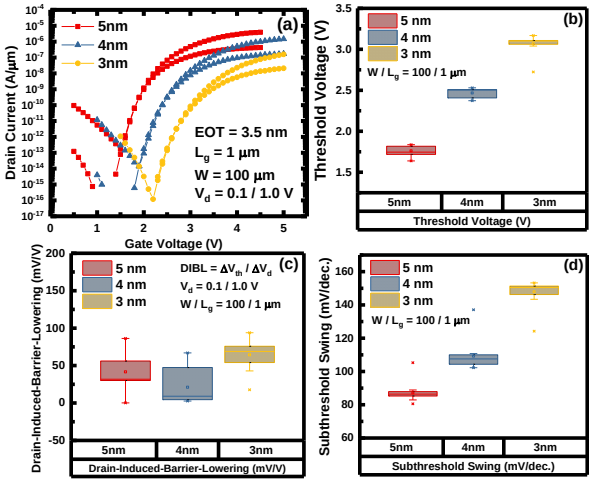

Fig.3 (a) Transfer characteristics of different T_{Si} device shows positive shift in V_{th} and greatly suppressed I_{off} with V_d = 1 V. (b) V_{th}, (c) DIBL, and (d) S.S. of T_{Si} 5/4/3 nm are compared. V_{th} shift can be infer from the highly doped channel. DIBL shows no difference. As oppose to common knowledge, S.S. degraded as T_{Si} scaled. S.S. might reflect the vertical crystallinity profile as we trim down the channel.

On-current (I_{on}), Off-current (I_{off}), and On/Off current ratio are shown in Fig.4. As T_{Si} is scaled, I_{on} [Fig.5 (a)] also decreases, which can be explained by the increase of channel resistance with smaller dimension, and severer interface scattering which in term reflects on degraded mobility in Fig.5 (a). Spreading resistance will add up to the series resistance in Fig.5 (b) as T_{Si} scaled and it will degrade I_{on} as well. On the bright side, I_{off} is greatly suppressed more than 2 orders of magnitude as shown in Fig.4 (b). The low leakage accomplished by channel trimming is suitable for low standby power application. In Fig.4 (c) we can see that I_{off} dominate the overall I_{on}/I_{off} ratio which reaches > 10^7 for 4 and 3 nm.

Vertical Crystallinity Profile

According to Haji and Le Borgne's separate works [5, 6], the closer the SPC poly-Si/oxide interface, the worse the crystallinity due to multiple nucleation site within few nanometers above the interface as illustrated in Fig.6. While this can be solved by improving gate electrostatic control with nanowire or gate-all-around structure, it gives us an insight into the channel quality within few nanometers thanks to the stable cyclic trimming process.

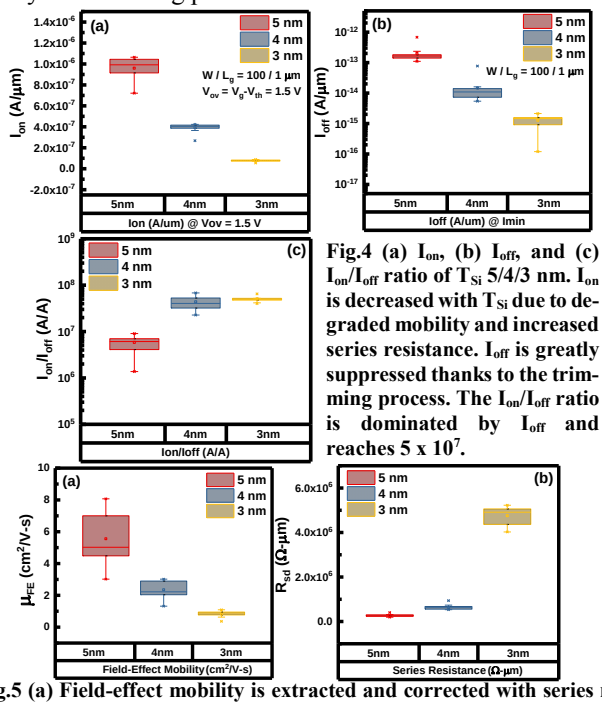

Fig.4 (a) I_{on}, (b) I_{off}, and (c) I_{on}/I_{off} ratio of T_{Si} 5/4/3 nm. I_{on} is decreased with T_{Si} due to degraded mobility and increased series resistance. I_{off} is greatly suppressed thanks to the trimming process. The I_{on}/I_{off} ratio is dominated by I_{off} and reaches 5 x 10^7.

Fig.5 (a) Field-effect mobility is extracted and corrected with series resistance. It degrades due to the severer surface scattering with thinner channel. (b) Normalized series resistance is extracted by total resistance method. As T_{Si} scaled, spreading resistance with further increase R_{sd} and degrade I_{on}.

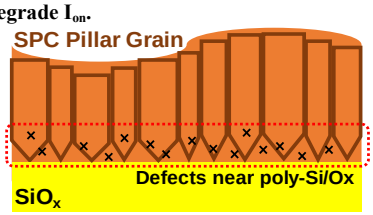

Fig.6 Defects near poly-Si/oxide interface are the multiple nucleation sites from SPC which are reflected by S.S. with each trimmed thickness.

4. Conclusion

Low temperature trimming process is developed to stably scale the junctionless device within nanoscale without surface degradation for low standby power applications. As T_{Si} is scaled to 3 nm, I_{on}/I_{off} and I_{off} reach $5x10^7$ and $1x10^{-15}$ (A/µm) respectively. The reversed S.S. behavior gives us an insight into the vertical crystallinity profile. The process show promising implementation in future nanosheet structure.

Acknowledgement

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