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Asymmetrical Voltage Driving for Memory Window Improvement of Flexible 1TFT-1RRAM Cells for Future Internet-of-Things Applications

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Abstract

In this paper, we propose a measurement scheme to improve the memory window (MW) of flexible Resistive Random Access Memory (RRAM) cells. The TaOx-based RRAM cell analyzed in this work is monolithically integrated with an amorphous InGaZnO-based thin-film transistor on a polymeric substrate using low-temperature fabrication process. By means of asymmetrical voltage driving during the set and reset phases, the RRAM cell yields a MW of 24, averaged over 50 set-reset cycles.

1. Introduction

Even though the thin-film-transistor (TFT) technology emerged relatively recently compared to the standard Si CMOS technology, it has already paved its way into consumer electronics, aiming for applications where TFT technology outperforms its CMOS counterpart in terms of size, cost or flexibility. The most prominent example of TFT dominance is the display industry [1]. Other application examples are large-area imagers, radio frequency identification smart tags and a simplified version of a microprocessor [2, 3].

Many potential applications envisioned in the frame of future internet-of-things devices require a memory component alongside a transistor, preferably a non-volatile type. Due to this interest, different concepts for the development of such a component have been studied [4], amongst others a Resistive Random Access Memory (RRAM) cell was proposed [5]. The previously published RRAM cell was monolithically integrated in a single fabrication process alongside a metal-oxide amorphous InGaZnO (a-IGZO) TFT which was used to select and source current to the memory element.

The aim of this work is to improve the memory window (MW) of the previously reported RRAM devices as one of its crucial figures of merit in order to enable more simplified readout circuitry. The larger MW was achieved by means of an alternative measurement procedure stemming from better understanding of the TFT technology properties during simultaneous functioning of both elements, the TFT and the RRAM.

2. 1TFT-1RRAM integration and TFT properties

For the 1TFT-1RRAM integration, a standard self-aligned a-IGZO TFT architecture was chosen. Its benefits are simplicity, requiring only four photolithography masks, while featuring good performance by avoiding overlapping parasitic capacitance between the gate and source/drain (S/D) contacts. The four photolithography masks mentioned define the semiconductor, followed by the gate and finished by the S/D via and metal patterning. In parallel with this process, three additional photolithography steps define the TaOx-based RRAM element: memory cell via, memory layer patterning and the routing metal. The RRAM size in this work measures 5 µm x 5 µm. More details on the design and fabrication process are available in [5]. Fig. 1 shows schematic and cross-section of 1TFT-1RRAM devices.

The minimal channel length of the fabricated TFTs is 5 µm and the devices show good uniformity over the full substrate. The mean threshold voltage amounts to V_{th} = -0.3 V with the standard deviation of 150 mV. The mobility of the fabricated a-IGZO TFTs approximates to 10 cm^2/Vs.

3. Asymmetrical voltage driving

While having the same metal-oxide-semiconductor structure, the a-IGZO TFT differs significantly from its standard Si counterpart. The first striking difference lies in the mobility, while the second stems from the a-IGZO TFT being a depletion type of the device with a slightly negative V_{th}. These differences can have obvious consequences when the a-IGZO TFT and the RRAM element operate together. Namely, from the shape of the programming curve during the set phase shown in Fig. 2 (a) it can be concluded that the TFT operates in the linear regime and never reaches saturation which would be a true benefit of having transistor as a driving element for RRAM. When voltage is kept symmetrical during set and reset phase, the V_{DS} applied is not high enough to fulfill the saturation requirement given by eq. (1).

$$|V_{DS}| \geq V_{GS} - V_{th} \quad (1)$$

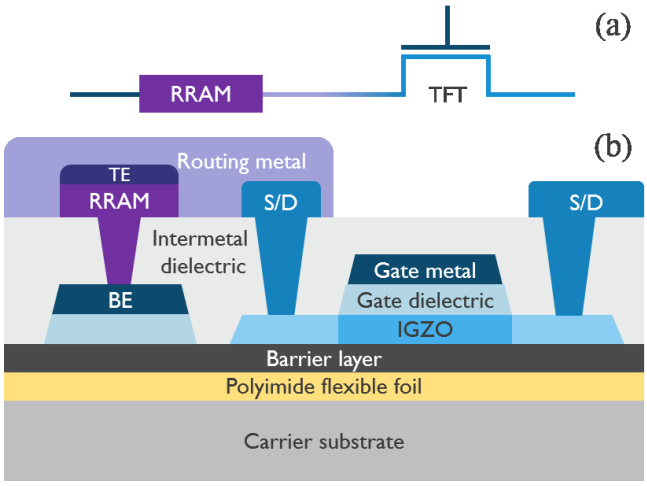

Fig. 1 (a) 1TFT-1RRAM cell schematic, (b) 1TFT-1RRAM cross-section.

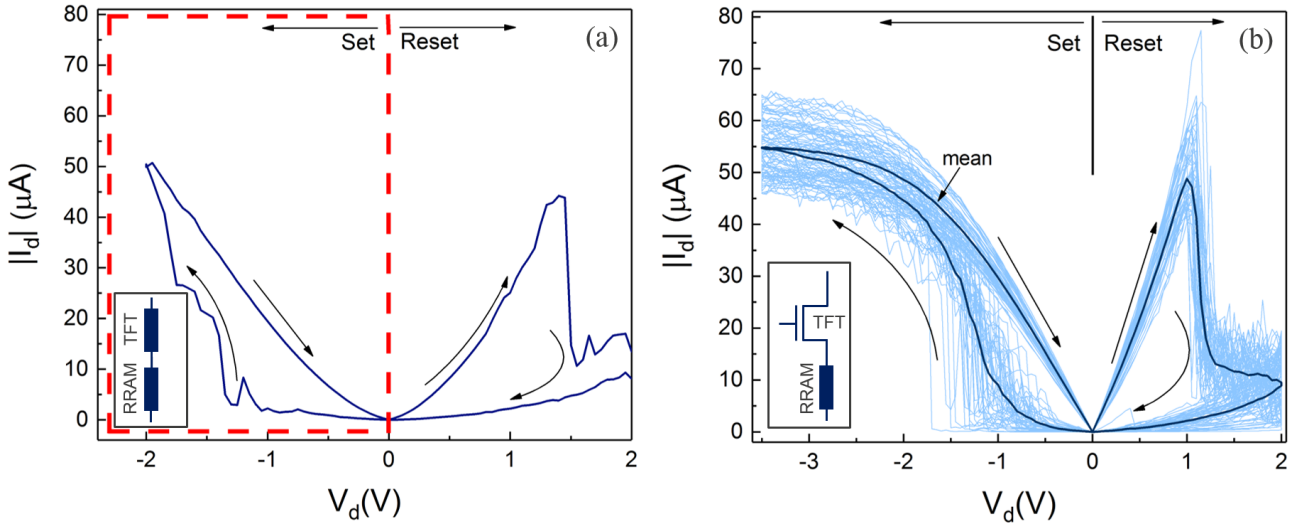

Fig. 2 (a) 1TFT-1RRAM set-reset curve using symmetrical voltage driving, (b) 1TFT-1RRAM during 50 set-reset cycles using asymmetrical voltage driving.

This is because the lower mobility of a-IGZO TFTs dictates the need for higher V_{GS} to provide enough switching current, while the depletion mode of n-type devices provides negative V_{th}, increasing even further the right part of the expression. Inset of Fig. 2 (a) indicates that in this case, the 1TFT-1RRAM device resembles a series connection of two resistors.

The asymmetrical voltage driving measurement scheme proposed in this work considers previous arguments and employs V_d voltage sweep of higher magnitude during the set with respect to the reset phase. In addition, the choice of a large TFT size of 840 µm / 5 µm (W/L) allows for V_{GS} reduction during the set phase while providing sufficient switching current. Consequently, the TFT can enter the saturation region, lowering its output resistance thus providing higher voltage for resistance manipulation of the memory element. The memory oxide filament created in this fashion is potentially more stable. The changes induced by the proposed voltage driving can help to enlarge the MW during the reset phase.

The asymmetric measurement scheme for flexible 1TFT-1RRAM devices consists of a negative V_d voltage sweep from 0 V to -3.5 V with V_{GS} of 3.2 V during the set phase to allow TFT saturation, and a positive V_d voltage sweep from 0 V to 2 V with V_{GS} of 8 V during the reset phase, while the source node was kept grounded. Fig. 2 (b) shows the raw data of 50 consecutive set-reset cycles of a 1TFT-1RRAM cell using the programming method proposed in this work. The mean curve of these 50 cycles is given for clarity. The average MW calculated as the current ratio between the low resistive and the high resistive state taken at $V_d = 0.5$ V amounts to 24, while cycles having MW > 100 are excluded. This result presents a MW improvement of at least a factor of 2 when compared to the first 50 cycles obtained by symmetrical voltage driving [5]. Fig. 3 shows the evolution of this current in both memory states along all the cycles.

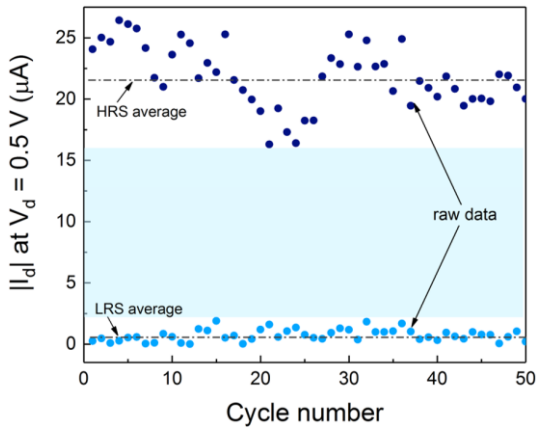

Fig. 3 Memory window along all cycles: HRS – high resistance state, LRS – low resistance state.

4. Conclusion

In this work, an asymmetric voltage driving measurement routine is proposed which accounts for specificity of the TFT technology when combined with the RRAM memory element. Higher magnitude of V_d during the set phase enables TFT saturation which can provide a more stable filament formation. The memory cell programmed in this manner provides larger MW compared to the symmetrical voltage driving, yielding a MW of ~24 over 50 set-reset cycles.

Acknowledgements

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