Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp331-332

Characteristics Variations and Reliability of CAAC-IGZO FETs

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Abstract

A field-effect transistor (FET) using c-axis-aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) in a channel layer (CAAC-IGZO FET) exhibits an extremely low off-leakage current and undergoes no change in mobility even in high-temperature environments. We fabricated a CAAC-IGZO FET with a trench gate self-aligned structure, and obtained small characteristics variations and high reliability. The FET with channel width/channel length = 60/60 nm achieved a variation in shift voltage σ = 64 mV, and 100 mV or less even after 490 h of a positive gate bias temperature test as a reliability test.

1. Introduction

Large-scale integration (LSI) for artificial intelligence, memory, central processing units, and field-programmable gate arrays has been actively researched and developed, but these devices have a problem of high power consumption. Silicon (Si) has been employed for the LSI to date; in recent years, LSI with a field-effect transistor using c-axis-aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO FET) has been increasingly reported[1–4]. The CAAC-IGZO FET has a unique feature of a low off-leakage current[5] and no change in mobility[6] even in high-temperature environments. Thus, aiming for low-power LSI, miniaturization of CAAC-IGZO FETs has been advanced. For LSI applications, the control of characteristics variations and reliability is required in addition to the miniaturization.

We fabricated a CAAC-IGZO FET employing a trench gate self-aligned (TGSA) structure, which is advantageous in miniaturization[7, 8]. This study reports the results of measuring the characteristics variations and reliability of the CAAC-IGZO FET with a channel width (W)/a channel length (L) = 60/60 nm.

2. Device Structure and Process Flow

Figure 1 shows a conceptual diagram and cross-sectional scanning transmission electron microscope (STEM) images of our fabricated FET with a TGSA structure. Figure 2 shows a process flow for fabricating the IGZO FET with a TGSA structure. The FET includes a back gate electrode (TiN＼W) that allows controlling the shift voltage (V_{sh})[9]. Separation of source and drain electrodes and formation of a buried gate (TiN＼W) region are made in a self-aligned manner. The FET has a size of W/L = 60/60 nm. The equivalent oxide thickness (EOT) of a gate insulating film is 5.6 nm. As shown in the cross-sectional STEM image in the W direction of Fig. 1(b), sides of the CAAC-IGZO are covered by a gate electrode, so that the FET is controlled by the gate electrode more effectively. Figure 3 shows the crystallinity in a channel region of the FET. Its clear layered structure indicates that the channel region surely includes CAAC-IGZO.

The IGZO FET can be stacked on a substrate provided with a Si metal oxide semiconductor FET. In addition, when IGZO FETs are stacked on each other, a space-saving device with a high density is achieved.

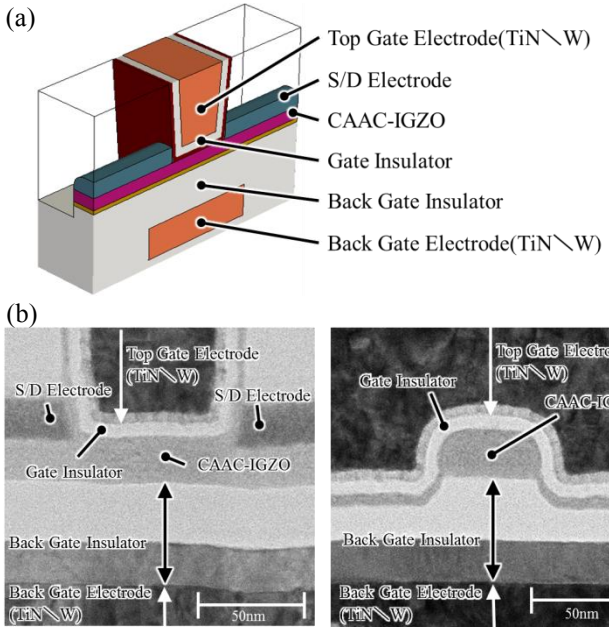

Fig. 1 (a) Schematic diagram of TGSA structure and (b) Cross-sectional STEM images (left: L-direction, right: W-direction).

- **Back gate electrode formation and gate insulator deposition**
- **IGZO deposition and island formation**
- **SiOx deposition and planarization by CMP**
- **S/D electrode formation in a self-aligned manner**
- **Top gate insulator deposition**
- **Top gate electrode formation**
- **Passivation and S/D electrode pad formation**

Fig.2 Process flow for fabricating IGZO FET with TGSA structure FET.

Fig.3 Cross-sectional TEM image of CAAC-IGZO

3. Characteristics of CAAC-IGZO FET

Figure 4 shows drain current-gate voltage (I_d-V_g) curves of our fabricated TGSA CAAC-IGZO FETs, and the normal probability distribution of the values is shown in Fig. 5. The V_{sh} is defined as V_g at an I_d of 10^{-12} A in the I_d-V_g curve with V_d = 1.2 V. A variation σ in V_{sh} of 215 devices each of which is designed to have W/L = 60/60 nm is 64 mV.

Since the V_{sh} of the CAAC-IGZO FET can be controlled with the back gate electrode, back gate voltage (V_{bg}) dependence of V_{sh} was measured. Figure 6 shows that V_{sh} can be shifted positively to 0.75 V when V_{bg} = −6 V. This is probably a noticeable effect produced when the CAAC-IGZO FET having a low off-leakage current is employed in LSI.

Next, a positive gate bias temperature test (PGBT) was performed on the same FETs and the amount of change in V_{sh} and a change in subthreshold slope (S.S.) over time were measured. In the PGBT, a stress of V_g = 3.63 V was applied at 150°C and the voltages of the source, the drain, and the back gate were each set to 0 V. As shown in the results in Fig. 7, the amounts of changes in V_{sh} and S.S. were within 100 mV and 10 mV/dec., respectively, after 490 h.

4. Conclusion

Minute FETs using CAAC-IGZO in channel layers were fabricated and their initial characteristics and reliability were evaluated. In the I_d-V_g curves of 215 FETs each with W/L = 60/60 nm, a variation in V_{sh} of 64 mV was achieved. In addition, the PGBT reliability test (at 150°C and V_g = 3.63 V) revealed that the amount of change in V_{sh} did not exceed 100 mV after 490 h. These results indicate that the TGSA CAAC-IGZO FET is applicable to actual operation of LSI.

References

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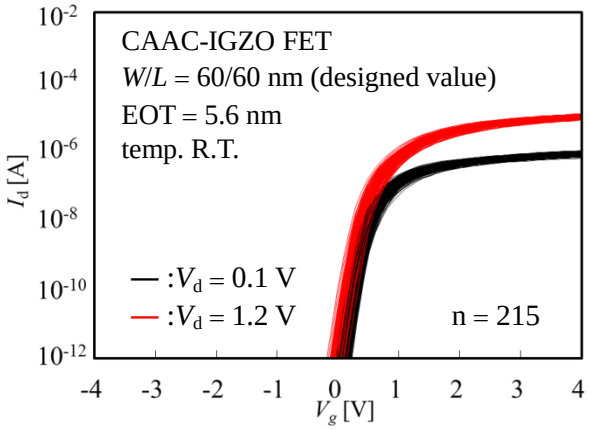

Fig. 4 CAAC-IGZO FET I_d-V_g curves

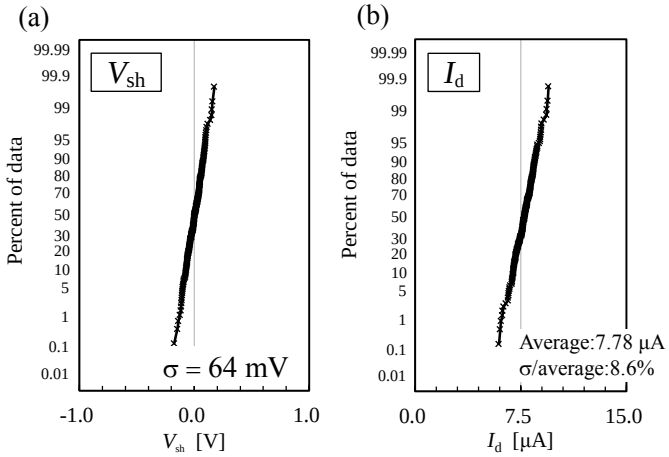

Fig. 5 CAAC-IGZO FET performance
・TEG: W/L = 60/60 nm (designed value) n = 215
(a) Normal probability plot V_{sh} at $I_d = 10^{-12}$ A
(b) Normal probability plot I_d at V_g = 3.3 V and V_d = 1.2 V

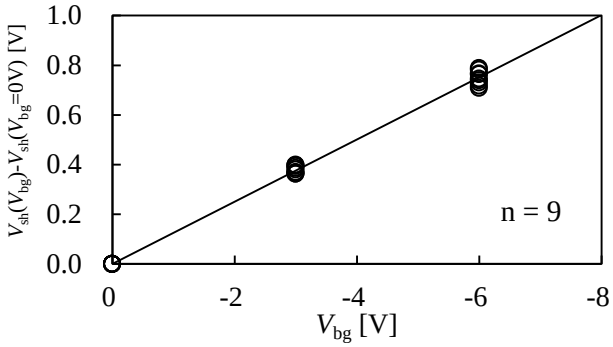

Fig. 6 V_{bg} dependence of V_{sh}

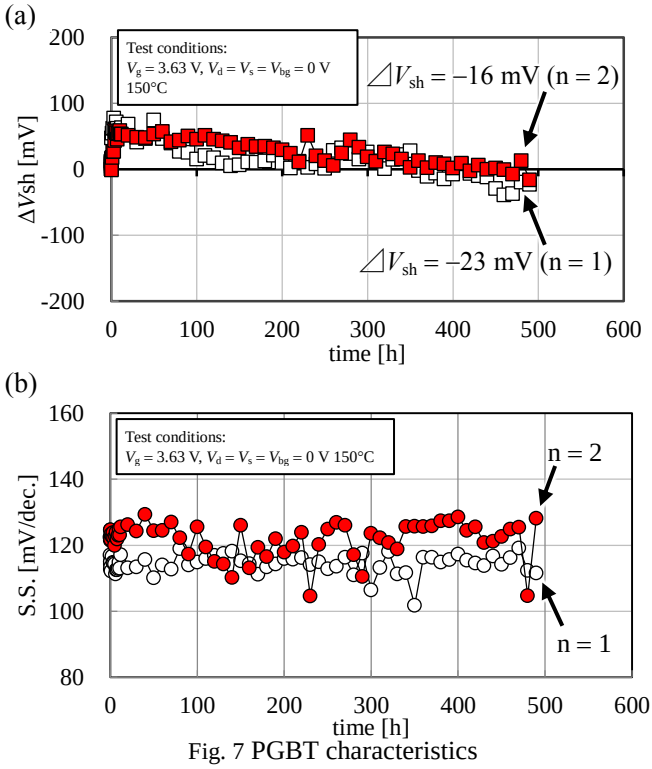

Fig. 7 PGBT characteristics
Test conditions: V_g = 3.63 V, V_d = V_s = V_{bg} = 0 V 150°C
(a) V_{sh}, (b) S.S. at V_d = 1.2 V