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5291-ppi OLED Display using CAAC-IGZO FET with Channel Length of 60 nm

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Abstract

FET using CAAC-IGZO can withstand relatively high voltages even when its channel length is 60 nm, which enables the use of this small FET in OLED pixels, leading to smaller pixels and, in turn, a high-resolution OLED display. For this work, we have designed, prototyped, and confirmed the operation of an OLED display (including peripheral circuits such as scan drivers) having over 5000 ppi.

1. Introduction

VR is increasing demand for a high-resolution display having over 3000 ppi[1]. However, displays with FETs on glass substrates have not yet been able to meet this demand[2].

The display industry recently has been active in research of FETs using oxide semiconductors (OS) in place of LTPS or a-Si:H, and the FETs using OS are in high-volume manufacturing. Research of OS began when Kimizuka, et al., synthesized IGZO approximately 30 years ago. Table I shows the classification of IGZO's crystallinity.

Table I Classification of IGZO

Amorphous [3,4]	"Intermadiate state" [5] / Novel boundary region [6] Crystalline	Crystal [13-15]
completely amorphous	・CAAC [7,8] ・nc [9-11] ・CAC [12] excluding single crystal and poly crystal	・single crystal ・poly crystal

CAAC-IGZO's carrier density is extremely low; thus, FETs using CAAC-IGZO (CAAC-IGZO FET) exhibit an extremely low off-state current on the order of yA (yoctoampere)/μm (10^{-24}/μm)[16]. This off-state performance of the CAAC-IGZO FET led to research in the LSI field for memory applications and the scaling of the CAAC-IGZO FET[17-19].

Typical scaled Si-CMOS devices are driven at low voltages and they are not designed to withstand voltages that FETs in display pixels typically encounter, such as over 5 V. For this work, we have designed, prototyped, and confirmed the operation of a high-resolution display using CAAC-IGZO FETs, which have high tolerance to higher voltages.

2. Pixel Circuit

Figure 1 is a circuit diagram of a 2T1C subpixel in the prototyped OLED display. In all subpixels, the select FET M1 is a CAAC-IGZO FET with a channel dimension of W/L = 60 nm/60 nm, and the drive FET M2 is a CAAC-IGZO FET with a channel dimension of W/L = 60 nm/200 nm. C1 is a storage capacitor.

The subpixels are arranged in a zigzag pattern because of the display's high resolution[20]. The subpixel pitch is 2.4 μm (H) × 3.2 μm (V), and all pixels that emit R, G, or B on the prototyped display have the same pitch between each other.

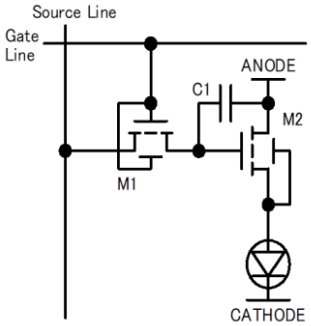


Figure 1 Subpixel circuit diagram.

3. Electrical Performance of CAAC- IGZO FET

Voltages used in the prototyped display was 5 V in the peripheral circuits and 8 V between anode and cathode. The performance of CAAC-IGZO FETs having the same size as those used as select or drive FETs (W/L = 60 nm/60 nm and W/L = 60 nm/200 nm) are shown in Figure 2.

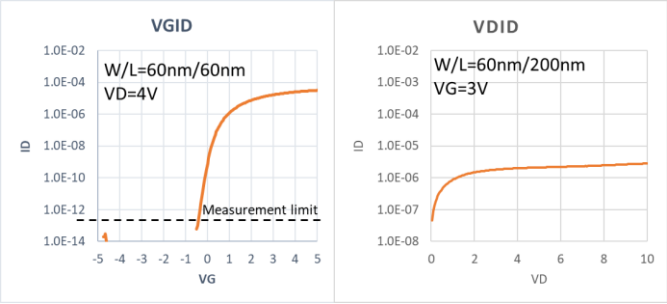


Figure 2 Performance of W/L = 60 nm/60 nm and W/L = 60 nm/200 nm CAAC-IGZO FET.

As shown in Figure 2 the gate of the select FET withstands more than 5 V and the drain of the drive FET withstands more than 10 V, confirming that the FETs can withstand voltages that are applied when displays are being driven.

4. Specifications and Display Operation

Figure 3 shows the configuration of the prototyped display. The resolution of the display is 1280 (H) × 720 (V). The scan drivers in the periphery of the pixels are all-n-type circuits made with CAAC-IGZO FETs, and are fabricated in the same fabrication process as the CAAC-IGZO FETs in the pixels. There are approximately 5 million FETs in the display, and the FET density on the display is 0.26 FETs/μm^2.

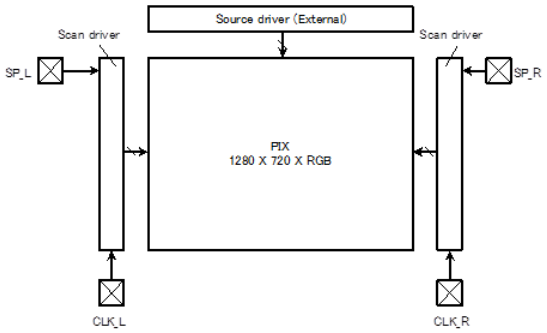


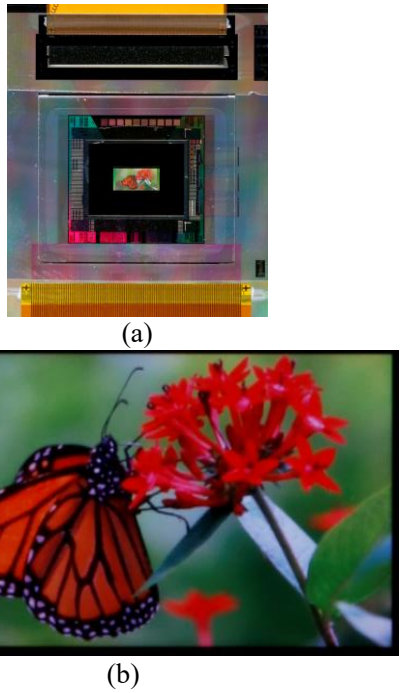
Figure 3 Display prototype configuration.

Table II lists the specifications of the prototyped display. It achieves a pixel density of 5291ppi by implementing small CAAC-IGZO FETs to shrink the subpixel pitch to 2.4 μm × 3.2 μm. In addition, we designed the display to accommodate 120 Hz operation, for demonstrating its feasibility in VR applications.

Table II Display specifications

	Specifications
Screen diagonal	0.28 inches
Resolution	1280 × 720
Subpixel pitch	2.4 μm × 3.2 μm
Pixel density	5291 ppi
Emission type	Top emission
Frame frequency	120 Hz
Source driver	External
Scan driver	Integrated

Figure 4(a) is a photograph of the prototyped display. The display region can be seen in the center and the scan drivers are placed by its sides. The size of the display region is 6.14 mm × 3.16 mm. The image displayed on the display region is enlarged in Figure 4(b). From Figure 4(b), it can be confirmed that the high-resolution display with over 5000 ppi, having CAAC-IGZO FETs (W/L = 60 nm/60 nm and W/L = 60 nm/200 nm) in pixels and peripheral circuits (e.g., scan drivers), displays an image properly.



(a)

(b)

Figure 4 (a) photo of the display prototype, and (b) image displayed on the display prototype.

5. Conclusion

A 5291-ppi, high-resolution display using CAAC-IGZO FETs (W/L = 60 nm/60 nm and W/L = 60 nm/200 nm) having high tolerance to high voltages was prototyped, and the display's proper operation was confirmed.

References

[1] K. Parikh, et al., SID Symposium. Digest, pp. 502-505 (2018).
[2] C.Vieri,et al., SID Symposium. Digest, pp. 5-8 (2018).
[3] K. Nomura et al., Nature, 432, pp. 488–492 (2004).
[4] T. Kamiya et al., Proc. IDW'13 Digest, pp. 280–281 (2013).
[5] E-mail that N. Kimizuka sent to M.Takahashi et al., on Sep. 8, (2012).
[6] Y. Waseda et al., Materials Transaction, 59, No 11 pp.1691-1700 (2018).
[7] S. Yamazaki et al., J. Soc. Info. Disp. 22, pp. 55-67 (2014).
[8] S. S. Yamazaki et al., Jpn. J. Appl. Phys., 53, 04ED18 (2014).
[9] S. Yamazaki et al., Japanese Patent No.5894694.
[10] S. Yamazaki et al., US Patent 9,153,650.
[11]S. Ito *et al.,* Proc. AM-FPD'13 Tech. Deg. Pap., p.151. (2013).
[12]S. S. Yamazaki et al., Jpn. J. Appl. Phys. 55, 115504 (2016).
[13]N. Kimizuka *et al.*, J. Solid State Chem., 60, pp.382-384 (1985).
[14]M. Nakamura et al., J. Solid State Chem., 93, pp.298-315 (1991).
[15]Y. Yamada *et al.* Jpn. J. Appl. Phys. 53, 091102 (2014).
[16]K. Kato, et al., Jpn. J. Appl. Phys. 51, 021201 (2012).
[17]A. Isobe et al., Symp. VLSI Circuit Dig.Tech.pp. 49-50 (2014).
[18]H. Tamura et al., IEEE Micro, vol.34, No.6, pp. 42-53 (2014).
[19]T. Onuki et al., Jpn. J. Appl. Phys. 54, 04DD07 (2015).
[20]M. Shiokawa, et al., SID Symposium. Digest, 1209 (2016).