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# 3x Improved Set-voltage Variability of Cu Atom Switch with Split-electrode for Very Large Scale Integration

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**Abstract** **3x improvement of set-voltage ($V_{set}$) variability of Cu atom switches (ASs) is realized by a split-electrode. The split-electrode makes the switches parallel and the switch with the smallest $V_{set}$ is automatically selected to turn ON, resulting in smaller $V_{set}$ variability. The split-electrode of 2-in-1 without area-overhead successfully reduces 6σ of $V_{set}$ from 2.56V to 2.25V with an equivalent σVset=28mV. The developed split-electrode enables the large scale integration of ASs for embedded memory and FPGA used in ultra-low power SoC.**

## 1. Introduction

A nonvolatile SoC with IP-cores of embedded nonvolatile memory (eNVM) and field programmable gate array (eFPGA) [1,2] are desired because the higher performance with higher power efficiency is a key for IoT/Edge-systems (Fig.1). A Cu atom switch (AS) using a polymer-solid electrolyte (PSE) (Fig.2) [3] integrated on CMOS is used not only for the low-power eNVM but also routing switches for the low-power eFPGA [4]. To satisfy required functions in the SoC, couples of configurations of the ASs are proposed, 1T1R for memory, 1T2R for routing switch, and 2T4R for LUT memory [4]. For the further scaling of AS-FPGA, larger number of ASs is needed to be integrated (Fig.3) [5-7], in which a variability in set-voltage ($V_{set}$) of ASs should be kept small.

In this work, to improve the $V_{set}$ variability of ASs, we newly propose a split-electrode of Cu, in which the electrode makes switches parallel and the cell having the parallel switches is named as Self-Selected Smallest Set-voltage cell (4S-cell). We fabricate the split-electrode structures and carefully investigate switching characteristics of the 4S-cell.

## 2. Concept of split-electrode

To realize the small variability of the programming voltage, we focus on the tail bits at 6σ (Fig.4). To reduce the 6σ of $V_{set}$, the switches are connected in parallel in the single cell by using the split-electrode. When programming voltage is applied, the switch having the smallest $V_{set}$ turns to be ON-state (Fig.5), in which the smallest $V_{set}$ switch in parallel is automatically selected, lowering $V_{set}$. The parallel structure is realized by the split-electrode of Cu. To extract the effect of the split-electrode, a simulation is carried out. Simulated results show that distribution of $V_{set}$ decreases with increasing the number of the switches in parallel from 1 to 8 (Figs 6 and 7). The 6σ of $V_{set}$ decreases and slope of $V_{set}$ distribution becomes steeper in the 4S-cell. We fabricated three kinds of structures including two 2-in-1 4S-cells with keeping the same cell area since the cell area is defined by the area of top-electrode (Fig. 8). The type A is conventional structure with edge-shaped Cu electrode [4]. The type B and C have the split-electrode of Cu for making 2-in-1 4S-cell. The ASs are integrated in a 40nm-node CMOS (Fig. 9).

## 3. Results and discussion

Resistance of AS changes with a formation of Cu bridge in the PSE by applying voltage (Fig.10). Almost the same switching characteristics are obtained irrespective of the types of the cells. This result indicates that the thickness of bridge (filament) is sufficiently smaller than the area of the electrode and there is no effect on each basic switching characteristic.

To confirm the effect of the split-electrode on the $V_{set}$ variability, a 64kb-array is evaluated. The $V_{set}$ reductions of tail bit are observed in type B and C, which are split-electrodes of 2-in-1 (Fig.11). The 6σ of $V_{set}$ are extrapolated, 2.56V (type A), 2.37V (type B) and 2.25V (type C), respectively. The split-electrode successfully reduces the $V_{set}$ at 6σ. The 6σ of $V_{set}$ of type C is lower than that of type B. The larger edge (peripheral) length in type C makes $V_{set}$ small due to higher switching probability on the edge with the lighting effect [8]. For type A, a thickness of the PSE is intentionally changed to see the tradeoff relationship between $V_{set}$ and leakage current ($I_{off}$) (Fig.12). Type B and C show lower $V_{set}$ with lower $I_{off}$ than those in the trend of type A, which indicates that the 4S-cell is effective to reduce $V_{set}$ with keeping low $I_{off}$.

Next, we quantify the effect of 4S-cell by using an equivalent $\sigma V_{set}$, in which the equivalent $\sigma V_{set}$ is defined as a slope satisfies the 6σ of $V_{set}$ in a theoretical normal distribution (Fig. 13). The equivalent $\sigma V_{set}$ of type B and C are 48mV and 28mV, respectively, resulting in 3x improvement of the $V_{set}$ variability to type A. The developed split-electrode paves the way of ASs to apply for very large scale integration of nonvolatile SoC with Giga-bit scale.

At last, the AS of type C is integrated on a 40nm-node CMOS with nine layered Cu BEOL (Fig.14). No failure is observed in the ON-state atom switches of both type A and C for 1 hour at 260ºC (Fig.15).

## 4. Conclusions

For the first time, the split-electrode of the atom switch is successfully demonstrated. We confirm that the 6σ of $V_{set}$ is reduced to 2.25V without increment of the cell size. And, switching characteristics and reliability are not degraded. The 4S-cell having the split-electrode can be used for routing switch of nonvolatile FPGA, LUT memory and NVM, realizing high-density and low-power nonvolatile SoC.

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## References

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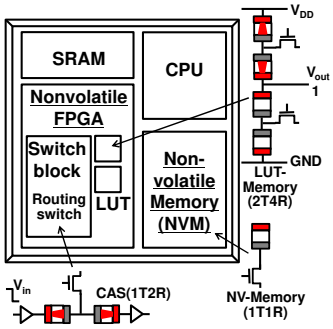


Fig. 1 Schematic view of nonvolatile SoC. Huge number of nonvolatile atom switches are integrated for eNVM and eFPGA.

Fig. 2 Schematic views of atom switch (AS).

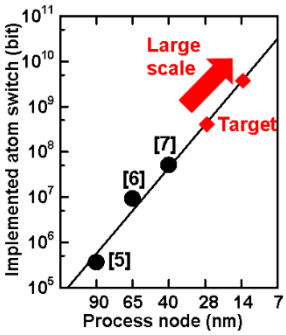


Fig. 3 Number of implemented ASs in programmable logic for each process node [5-7].

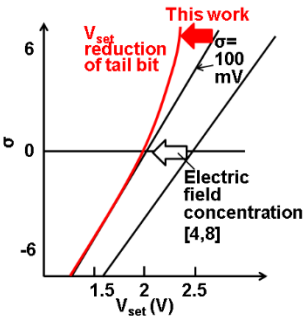


Fig. 4 Concept to reduce set-voltage ($V_{set}$) of ASs. To follow scaling, $V_{set}$ reduction of tail bit is needed.

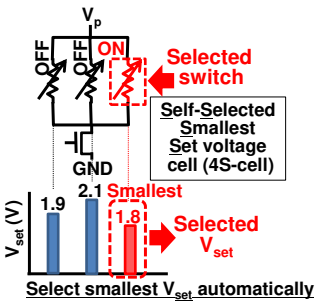


Fig. 5 Concept of proposed circuit structure of AS. By increasing number of switches, switch with smallest $V_{set}$ turns to ON-state automatically. It is named as 4S-cell.

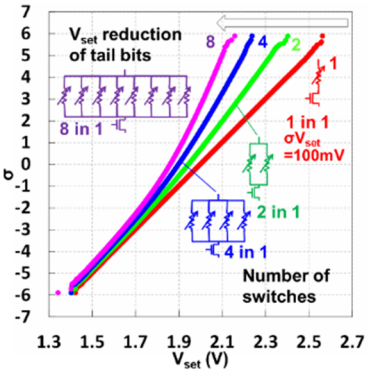


Fig. 6 Simulated distribution of $V_{set}$ for different number of switches in cell. $\sigma V_{set}$ of 1-in-1is 100mV.

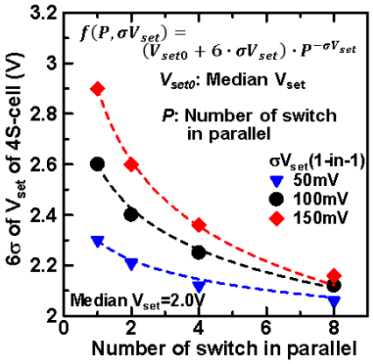


Fig. 7 Simulated 6σ of $V_{set}$ vs. number of switches in parallel with various $\sigma V_{set}$ of simple switch (1-in-1).

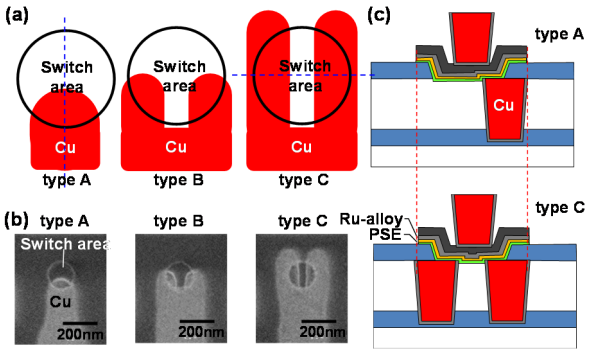


Fig. 8 (a) Schematic top views of split-electrode, (b) top SEM images and (c) schematic cross-sectional views of devices. All types have the same cell size.

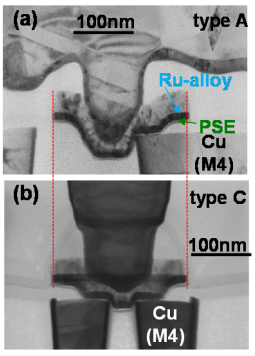


Fig. 9 Cross-sectional TEM images of (a) type A and (b) type C.

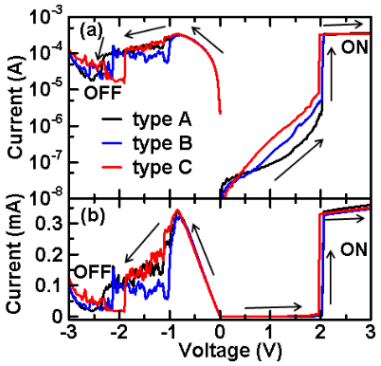


Fig. 10 Current-voltage characteristics for different electrode type. (a) Logarithmic plot. (b) Linear plot.

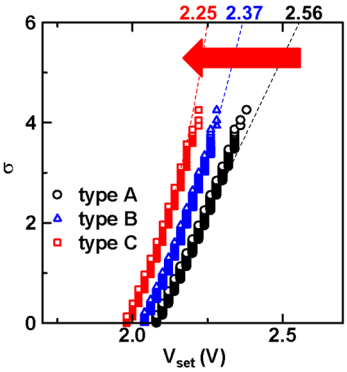


Fig. 11 Comparison with distributions of $V_{set}$ of type A, B, and C using 64kb-array. $V_{set}$ at 6σ reduces by the split-electrode effect.

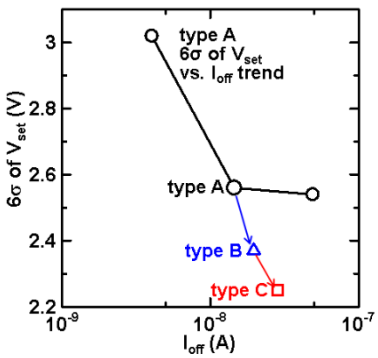


Fig. 12 6σ of $V_{set}$ vs. leakage current ($I_{off}$). In comparison with the $V_{set}$ vs. $I_{off}$ trend of type A, type B and C show low $V_{set}$ and low $I_{off}$. Read voltage is 0.4V.

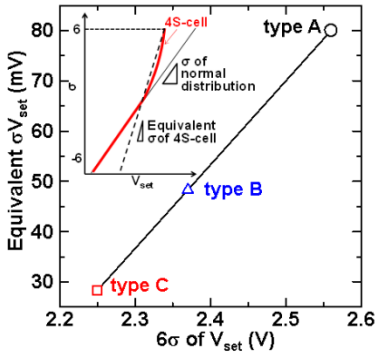


Fig. 13 6σ of $V_{set}$ vs equivalent $\sigma V_{set}$. $\sigma V_{set}$ of type B and C indicate 48mV and 28mV, respectively. 3x improvement of $V_{set}$ variability is achieved.

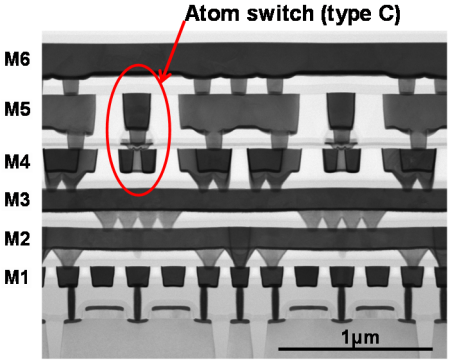


Fig. 14 Cross-sectional TEM image of integrated atom switch of type C on 40nm-node CMOS with nine layered BEOL.

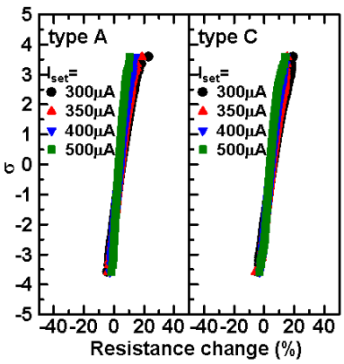


Fig. 15 Resistance change in ON-state of type A and C after retention test for 1hour at 260°C for various set-current ($I_{set}$).