Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp357-358

85% Endurance Error Reduction by Changing Reset Voltage in 40nm TaO_X-based ReRAM

Hiroshi Kinoshita[1], Shouhei Fukuyama[1], Tsubasa Yonai[1], Ryutaro Yasuhara[2] and Ken Takeuchi[1]
[1]Department of Electrical, Electronic and Communication Engineering, Chuo University, Tokyo, 112-8551, Japan
[2]Panasonic Semiconductor Solutions Co., Ltd., 1 Kotari-yakemachi, Nagaokakyo, Kyoto, 617-8520, Japan
E-mail: hiroshi.kinoshita@takeuchi-lab.org

***Abstract* — This paper proposes Changing Reset Voltage technique for 40nm TaO_X-based resistive random access memories (ReRAM). The proposed technique changes Reset voltage (V_{RESET}) at the high endurance such as 10^4 Set/Reset cycles. Changing Reset Voltage technique decreases measured total Bit-Error Rate (BER) of both LRS and HRS by 85%, compared with conventional fixed Reset voltage. In addition, the current difference between LRS and HRS at probability = 50% increases by 57% with the proposal, which increases the read margin between Set and Reset. Finally, this paper proposes a physical model about proposed Reset.**

Introduction

Resistive random access memory (ReRAM) is attracting much attention for next generation non-volatile memories. However, ReRAM has reliability trade-off between Set/Reset cycles (endurance) and data-retention time (lifetime) [1, 5]. Recently, long-term lifetime is realized until 10^4 Set/Reset cycles [1]. This paper proposes Changing Reset Voltage technique to reduce the endurance errors and eventually to realize both high endurance and long-term data-retention lifetime.

Conventional Set/Reset Measurement

ReRAM stores "1" (Low Resistance State, LRS) and "0" (High Resistance State, HRS) as shown in Fig. 1. The oxygen vacancy (V_O)/oxygen ions (O^{2-}) inside conductive filament (CF) move between TaO_X layer and $Ta_2O_{5-\delta}$ layer by Set/Reset operation [2, 3]. Fig. 2 shows conventional Set/Reset. In this protocol, Set and Reset are repeated alternately. After that, DC cell current is measured at 10, 10^2, 10^3, 10^4, 10^5 and 10^6 cycles. In this paper, to investigate the worst case reliability, all measurements are performed at severe conditions which cause excessive stress. Fig. 3 shows the measured results at V_{RESET} = 1.1 (a.u.). Fig. 3(a) shows cumulative probability (CP) plots of cell current distributions of LRS and HRS. Fig. 3(b) shows total BER of both LRS and HRS. After 10^4 Set/Reset cycles, total BER abruptly increases [4]. Tail bit is the tail portion of the current distributions of LRS. Fig. 4 shows the measured results with conventional Set/Reset until 10^4 Set/Reset cycles at V_{RESET} = 0.6~1.6 (a.u.). V_{RESET} = 1.1 (a.u.) achieves the lowest total BER among all Reset voltages and thus is optimal.

Proposed Set/Reset Measurement and Discussion

Fig. 5 shows proposed Set/Reset. To improve reliability at the high endurance cycles, this paper proposes Changing Reset Voltage. In the conventional protocol, V_{RESET} is fixed throughout the entire Set/Reset cycles. On the other hand, in the proposed Set/Reset, V_{RESET} is changed after 10^4 Set/Reset cycles. Fig. 6 compares measured results of conventional and proposed Set/Reset at V_{RESET} = 0.6~1.6 (a.u.). Fig. 6(a) shows measured results with conventional Set/Reset until 10^6 Set/Reset cycles. Fig. 6(b) shows the measured results of proposed Changing Reset Voltage technique. V_{RESET} = 1.1 (a.u.) is applied until 10^4 Set/Reset cycles and after 10^4 Set/Reset cycles V_{RESET} is reduced. In this measurement, after 10^4 Set/Reset cycles, the optimal voltage is V_{RESET} = 0.6 (a.u.). In other words, the optimal write voltage is V_{RESET} = 1.1 (a.u.) until 10^4 Set/Reset cycles and after that changes to V_{RESET} = 0.6 (a.u.). As shown in Fig. 7, Changing Reset Voltage has two benefits. First, Changing Reset Voltage decreases tail bits. Second, Changing Reset Voltage increases the current difference between LRS and HRS at probability = 50%. Because the read margin between Set and Reset increases, the number of error cells during the read decrease. Fig. 8 shows comparison of total BER between proposed and conventional Set/Reset. At 10^6 Set/Reset cycles, total BER of the proposed Changing Reset Voltage decreases by 85%. From Figs. 6-8, proposed Changing Reset Voltage is effective at high endurance cycles. Furthermore, proposed technique reduces power consumption during Reset by reducing Reset voltage and does not change writing speed. Finally, a physical model of LRS is proposed in Fig. 9. CF expands crosswise as Set/Reset cycling increases in conventional Set/Reset [2, 5]. Consequently, percolation path is cut off at high endurance [6]. On the other hand, proposed Changing Reset Voltage suppresses crosswise expansion of the filament and suppresses reduction of the oxygen vacancy density inside the filament because of lower write voltage at the high endurance. As a result, cut-off of the percolation path is suppressed by Changing Reset Voltage protocol at the high endurance, which reduces the tail bits of LRS. In addition, because the voltage balance between Set and Reset changed after Reset voltage changed at 10^4 Set/Reset cycles, characteristics of the conductive filament has also changed. As a result, distributions of both HRS and LRS shifts to the higher current direction and thus the margin between HRS and LRS increases.

Conclusion

This paper experimentally demonstrates that proposed Changing Reset Voltage decreases total BER by 85% at 10^6 Set/Reset cycles. Moreover, Changing Reset Voltage increases the current difference between LRS and HRS at probability = 50% increases by 57%. In addition, Changing Reset Voltage reduces power consumption at the high endurance because V_{RESET} is reduced from 1.1 to 0.6 (a.u.). Furthermore, the proposed Set/Reset does not change write speed. Thus, at the high endurance cycles, this proposal is quite effective.

Acknowledgment

The authors would like to thank A. Hayakawa, C. Matsui, K. Kamimura and R. Kinoshita for their support. This work was partially supported by CREST, JST, Grant Number JPMJCR1532, Japan.

References

[1] S. Fukuyama *et al.,* in *IRPS,* pp. 7C.3.1-7C.3.6, 2019.
[2] T. Ninomiya *et al., TED*, vol. 60, no. 4, pp. 1384-1389, 2013.
[3] Z. Wei *et al.,* in *IEDM Tech. Dig.*, pp. 293-296, 2008.
[4] A. Hayakawa *et al.,* in *IMW*, pp. 24-27, 2017.
[5] S. Fukuyama *et al.,* in *NVMTS*, pp. 1-4, 2018.
[6] K. Maeda *et al.,* in *IRPS*, pp. 5A-4.1-5A-4.6, 2017.

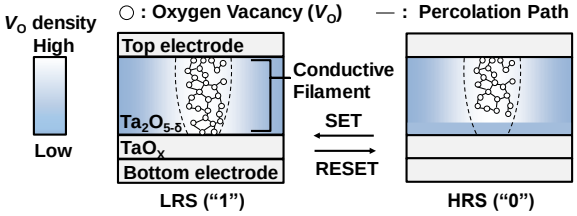

Fig. 1 Conduction switching of TaO_X-based ReRAM device [2, 3].

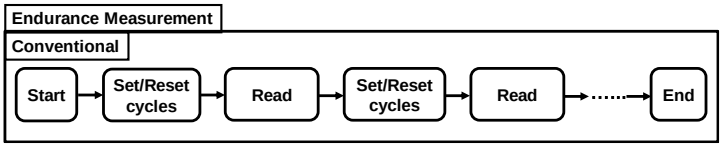

Fig. 2 Protocol of conventional Set/Reset measurement. At first, Set/Reset endurance cycles are measured at constant Reset voltage, V_{RESET} = 0.6~1.6 (a.u.). Set voltage, V_{SET} is fixed in all measurement.

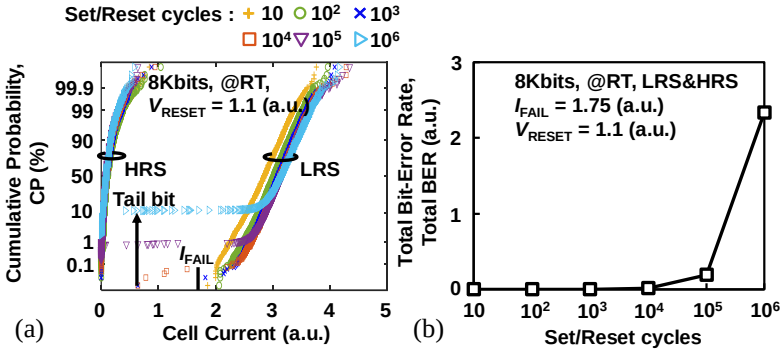

Fig. 3 (a) Measured current distribution in case of V_{RESET} = 1.1 (a.u.) and (b) total Bit-Error Rate (BER) of both LRS and HRS in conventional Set/Reset.

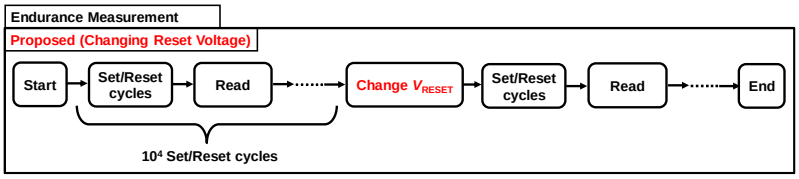

Fig. 5 Protocol of proposed Set/Reset measurement. At first, Set/Reset cycles are measured by changing V_{RESET}. V_{SET} is fixed in all measurement. After 10^4 Set/Reset cycles, V_{RESET} is changed.

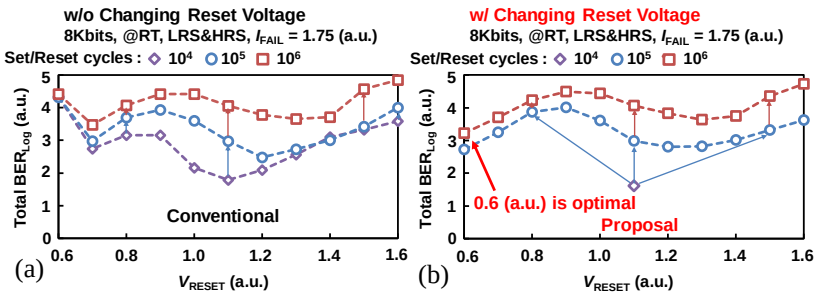

Fig. 6 (a) Measured endurance characteristics of V_{RESET} = 0.6~1.6 (a.u.) without Changing Reset Voltage (Conventional) and (b) with Changing Reset Voltage (Proposal).

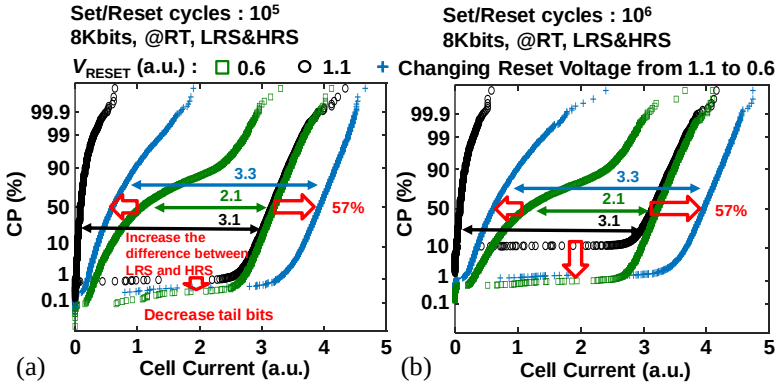

Fig. 7 Measured current distribution in case of fixed V_{RESET} = 0.6 (Conventional), 1.1 (Conventional) and Changing Reset Voltage from 1.1 to 0.6 (Proposal) at (a) 10^5 and (b) 10^6 Set/Reset cycles.

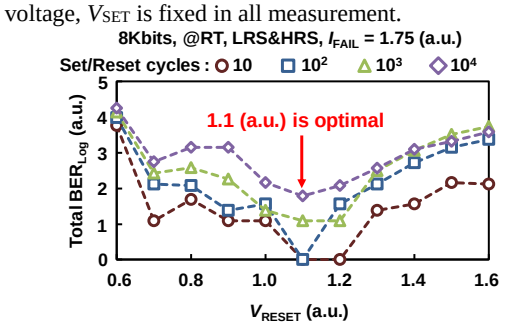

Fig. 4 Measured endurance characteristics of V_{RESET} = 0.6~1.6 (a.u.) until 10^4 Set/Reset cycles with conventional Set/Reset.

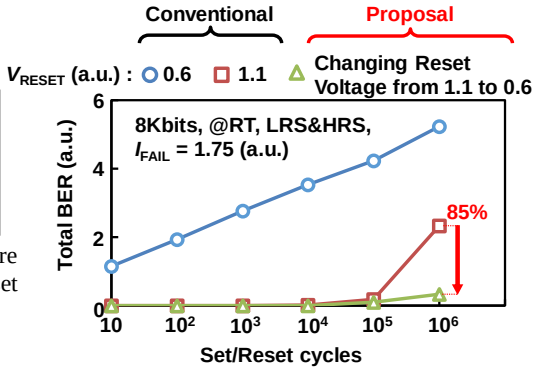

Fig. 8 Comparison of conventional and proposal Set/Reset measurement. Total BER of LRS and HRS decreases by 85% with Changing Reset Voltage at 10^6 Set/Reset cycles.

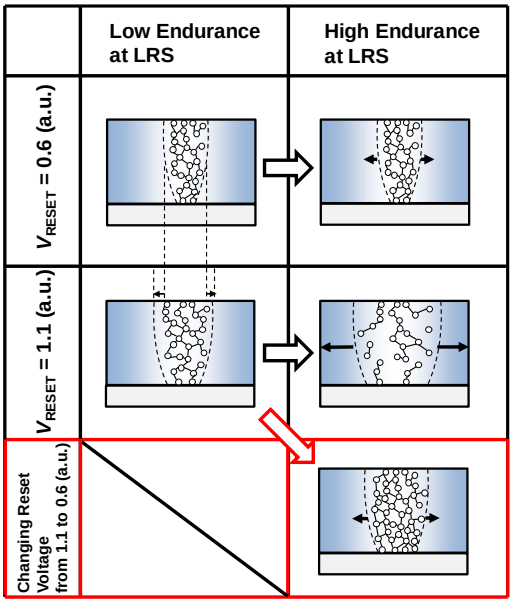

Fig. 9 Physical model of endurance stress of LRS. Proposed Changing Reset Voltage suppresses the reduction of the oxygen vacancy and its expansion crosswise.