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Interface dipole modulation in ALD HfO_2/SiO_2 multi-stack MOS structures

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Abstract

We first demonstrated interfacial dipole modulation (IDM) in HfO_2/SiO_2 stack structure fabricated by atomic layer deposition (ALD). Electrical and physical characteristics of the ALD-IDM structures are presented in this paper. We also found that the ALD temperature largely affects the IDM operation.

1. Introduction

A new memory operation based on HfO_2/SiO_2 gate stack which we call interface dipole modulation (IDM) has been proposed [1]. This potential switching is considered to be originated from electric-field-induced atomic displacement around the interface 1-monolayer (ML) TiO_2, and this memory device offers advantages as a low-temperature process of gate stack structure, compared with the ferroelectric HfO_2 memory [2]. However, in previous work, a high-vacuum EB-evaporation method unsuitable for mass production has been used to deposit oxide layers. In this study, we examined the applicability of atomic layer deposition (ALD) method to fabricate HfO_2/SiO_2 IDM MOS structure.

2. Experimental

Deposition of HfO_2, TiO_2, and SiO_2 layers was performed using metal-organic precursors and O_2 plasma at 150-350°C in the same ALD reactor. The $HfO_2/TiO_2/SiO_2$ multi-stack structure was fabricated on SiO_2-coverd p-type Si substrate. ALD cycles of the interfacial TiO_2 were set at 4 times, which correspond to 0.16-nm-thick TiO_2 deposition under the standard ALD conditions. Post deposition annealing (PDA) was performed at 300 or 350°C in an O_2/Ar (~21%) atmosphere, and then Au electrodes were deposited on the oxide surface to fabricate the MOS capacitors. Figure 1 shows a TEM image observed from an ALD-prepared multi-stack MOS capacitor, indicating that a HfO_2/SiO_2 structure having a definite interface can be fabricated by our method. Note that interfacial TiO_2 cannot distinguish from SiO_2 in the TEM image.

3. Results and discussion

Figure 2 shows *C-V* curves observed from a multi-stack structure with six interface TiO_2 layers, which were prepared by 200°C-ALD and 300°C-PDA. The clockwise *C-V* hysteresis suggests a gate-induced potential change in the MOS structure. The *C-V* curve of the reference HfO_2/SiO_2 multi-stack sample without interface TiO_2 layer shows negligible hysteresis [Fig. 3]. We can reasonably conclude that the interface TiO_2 play a crucial role in the potential change.

Figure 4 shows the x-ray photoelectron spectroscopy (XPS) result for an IDM sample having uppermost 4-nm-HfO_2 layer. The Ti 2*p* and Si 2*p* photoelectron intensities are reasonably weak considering photoelectron attenuation in the uppermost HfO_2 layer. This XPS result exhibits that the main components of each oxide are HfO_2, TiO_2, SiO_2. The Ti depth profile of secondary ion mass spectroscopy (SIMS) shown in Fig. 5 shows that Ti atoms exist at around the HfO_2/SiO_2 interface even after the PDA at 350°C. According to these results and the above TEM image, we concluded that the $HfO_2/TiO_2/SiO_2$ stack, which is our intended structure, can be fabricated by ALD method. Thus, we consider that the potential change observed in the *C-V* curves corresponds to the interface dipole modulation induced by structural change around the interface TiO_2 as proposed for HfO_2/1-ML TiO_2/SiO_2 stack structure fabricated by an evaporation method [3].

Finally, we will discuss the effect of ALD temperature on IDM operation. Figure 6 shows a *C-V* curve of six-TiO_2 modulator sample prepared by 300°C-ALD, which shows counter-clockwise *C-V* hysteresis. This implies that trapping of holes injected from the silicon substrate into the oxide stack is dominant, compared to the IDM effect. Figure 7 compares two TiO_2 modulator samples prepared under different ALD temperature conditions and supports the IDM characteristics lost by high ALD temperature. Figure 8 summarizes the maximum V_{fb} shift (ΔV_{fb}) estimated by *C-V* measurements at 5 kHz under light illumination [1, 2]. There is an obvious boundary between 250°C and 300°C. Furthermore, even though the PDA temperature exceeds this boundary temperature, IDM operation is possible for low-temperature ALD samples. Therefore, we conclude that the oxide structure formed during the ALD process mainly determines whether IDM operation is possible or not.

4. Conclusions

We demonstrated IDM operation in ALD-prepared HfO_2/SiO_2 multi-stack structure with TiO_2 modulation layers. We found that ALD temperature has a large impact on the IDM operation rather than the PDA process.

Acknowledgements

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References

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[3] N. Miyata, J. Nara, T. Yamasaki, K. Sumita, R. Sano, and H. Nohira, IEEE International Electron Devices Meeting (IEDM), 7.6.1 (2018).

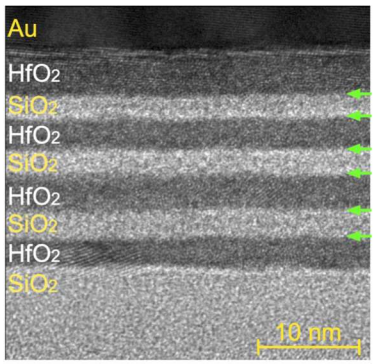

Fig. 1 TEM image of HfO_2/SiO_2 multi-stack structure prepared by ALD at 200°C. TiO_2 layer grown with 4 ALD cycles were inserted at the interface indicated by the arrow.

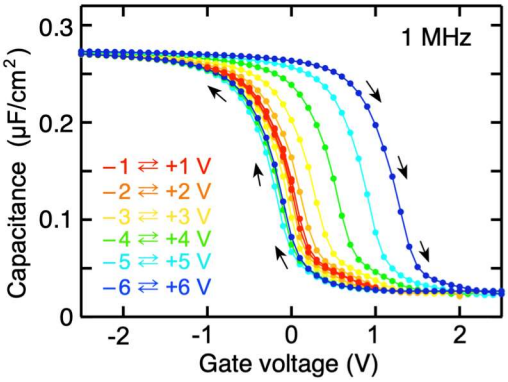

Fig. 2 *C-V* curves of multi-stack HfO_2/SiO_2 MOS with six TiO_2 modulation layers. Clockwise *C-V* hysteresis suggests a potential change by IDM.

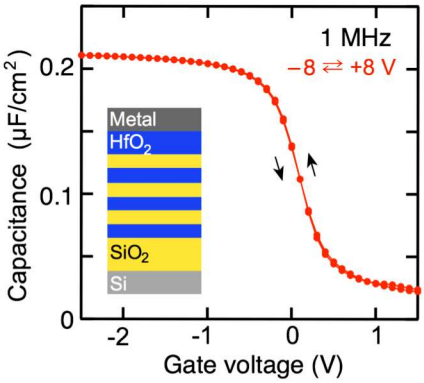

Fig. 3 *C-V* curve of multi-stack HfO_2/SiO_2 MOS without interface TiO_2 layer. *C-V* hysteresis is negligible.

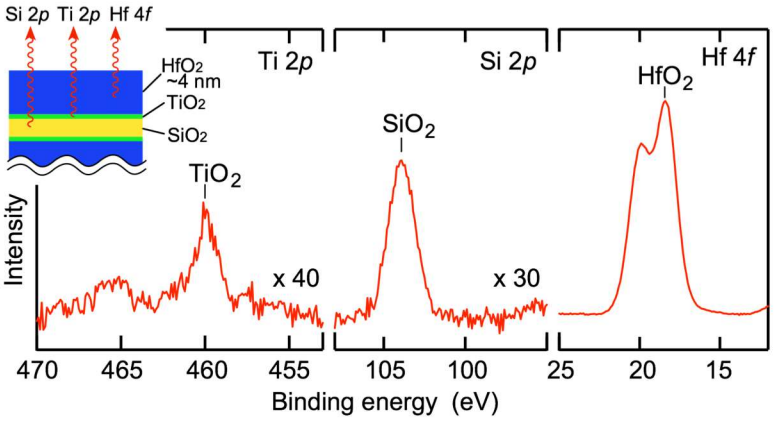

Fig. 4 Ti 2*p*, Si 2*p*, and Hf 4*f* photoelectron spectra of a multi-stack structure with an uppermost 4-nm-HfO_2 layer. The main oxide components are assigned to stoichiometric TiO_2, SiO_2, and HfO_2.

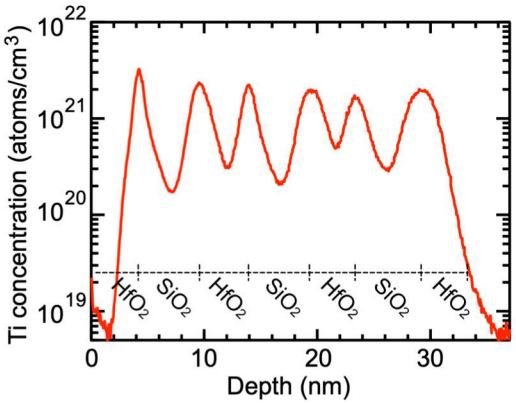

Fig. 5 SIMS depth profile of Ti concentration in 5-nm-HfO_2/5-nm-SiO_2 multi-stack structure. Ti atoms exist at around the HfO_2/SiO_2 interface.

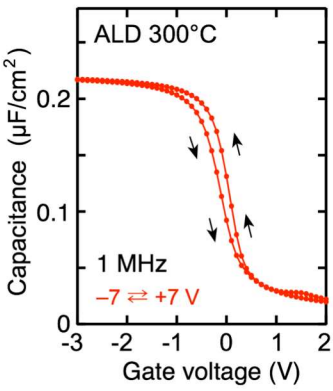

Fig. 6 *C-V* curve of MOS capacitor with six TiO_2 modulation layers prepared by ALD at 300°C.

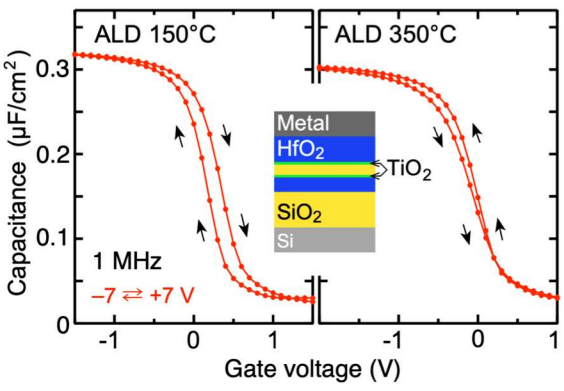

Fig. 7 *C-V* curves of MOS capacitors with two TiO_2 modulation layers. Hysteresis rotation depends on ALD temperature.

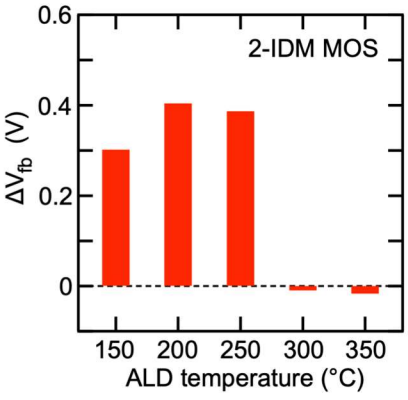

Fig. 8 Effect of ALD temperature on maximum V_{fb} shift (ΔV_{fb}) of two TiO_2 layer samples. High temperature ALD samples lose the IDM characteristics.