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Nanocrystal-Embedded-Insulator (NEI) Ferroelectric FET Based synapse for neuromorphic network

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Abstract

A novel nanocrystal-embedded-insulator (NEI) ferroelectric field-effect transistor (FeFET) is demonstrated to mimic as a synaptic device for analog neural network (NN) applications. The NEI layer (down to 3.6 nm in thickness) consisting of ZrO_2 nanocrystals embedded in amorphous Al_2O_3, demonstrates the reduced operating voltages compared to doped-HfO_2 films. NEI FeFET synapse achieves very small weight update non-linearity (α_p/α_d=0.08/0.10) and asymmetry factors, advantageous for analog-style NNs with online training. A CNN is designed and emulated for a MNIST dataset, projecting an online training accuracy of 94%.

1. Introduction

Polycrystalline doped-HfO_2 (*e.g.* HfZrO, Si:HfO_2) ferroelectric field-effect transistors (FeFETs) have attracted considerable interest for neuromorphic synapse applications due to their compact device structure and CMOS process compatibility [1, 2]. However, scaling to thicknesses below 5 nm results in undesired gate leakage current and degradation of the ferroelectric materials [1, 3, 4]. By incorporating a "Nanocrystal-Embedded-Insulator" (NEI) ferroelectric film in gate stack, FeFET can operate at a lower voltage and mitigate depolarization issues [5].

In this work, NEI FeFET for synaptic behavior is experimentally demonstrated. Analog neural networks (NN) using a sign back-propagation (SBP) algorithm are then emulated to investigate the impact of synaptic device performance on NN online training accuracy.

2. Device Fabrication and Ferroelectric Properties

The key process steps for NEI FeFET fabrication is illustrated in Fig. 1(a). 4-inch n-type Ge(001) wafer was used as the starting substrate. After pregate cleaning using diluted HF, Ge(001) wafer was loaded into an atomic layer deposition (ALD) chamber for the deposition of the 3.6 nm NEI layer comprising ZrO_2 nanocrystals embedded in amorphous Al_2O_3 amorphous matrix. TaN metal gate was deposited using the reactive sputtering. After the gate formation, BF_2^+ ions were implanted into the source/drain regions. 30 nm nickel (Ni) was deposited in source/drain regions using the lift-off process. Finally, device fabrication was completed with rapid thermal annealing (RTA). Fig. 1(b) shows the 3D schematic of the fabricated NEI FeFET.

Fig. 1(c) indicates the thicknesses of the NEI is 3.6 nm. High-resolution TEM (HRTEM) image in Fig. 1(d) demonstrates the ZrO_2 nanocrystals embedded in amorphous Al_2O_3 on Ge(001) in the NEI sample. Based on the diffraction

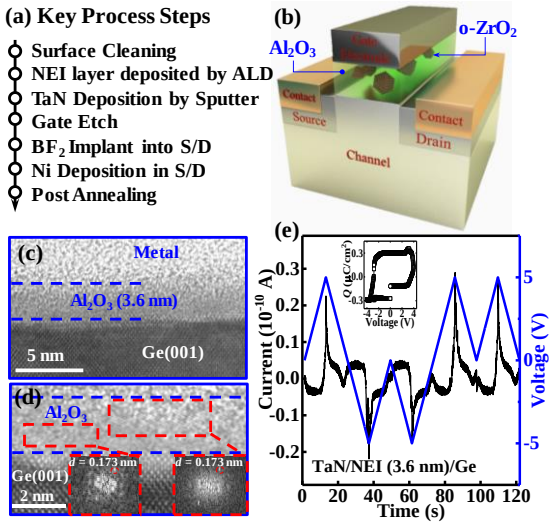

Fig. 1 (a) Key process steps for fabricating NEI FeFET. (b) 3D schematic of NEI FeFET. (c) XTEM images of the gate stack of FeFET with 3.6 nm NEI layer. (d) HRTEM image showing nanocrystals embedded in amorphous Al_2O_3 for the sample. (e) PUND test of TaN/NEI(3.6 nm)/Ge capacitor, and the insert is the extracted *Q* - *V* loop.

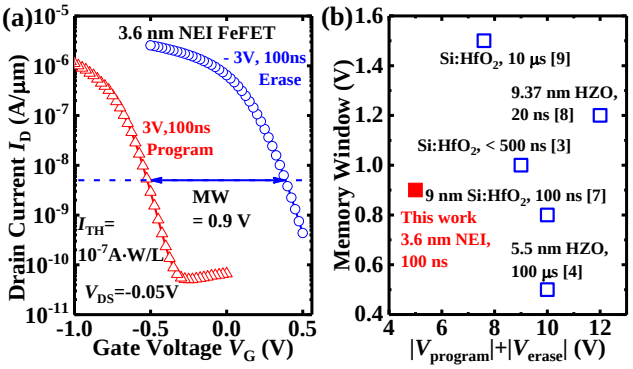

Fig. 2. (a) I_D - V_G characteristics from a 3.6 nm NEI FeFET for the two polarization states with 100 ns program/erase pulses. (b) Benchmarking of NEI FeFET memory with reported HfO_2-based FeFETs on to MW and $V_{program}$+|V_{erase}|. NEI FeFET achieves low operating voltages while maintaining decent MW.

patterns, the interplanar spacing *d* within the nanocrystals is calculated to be 0.173 nm, corresponding to (111)-oriented orthorhombic ZrO_2 phase [6]. The polarization of the 3.6 nm NEI gate stack was characterized using the positive-up-negative-down (PUND) technique [Fig. 1(e)].

3. Results and Discussion

Fig. 2(a) shows measured I_D-V_G characteristics for a 3.6

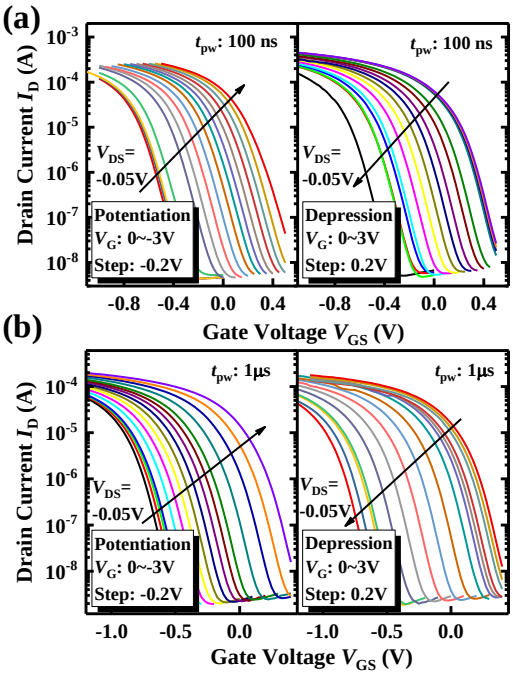

Fig. 3 NEI FeFET synapse behaviors: gradual tuning of I_D - V_G curves under (a) 100 ns and (b) 1 µs voltage pulses for potentiation and depression operations.

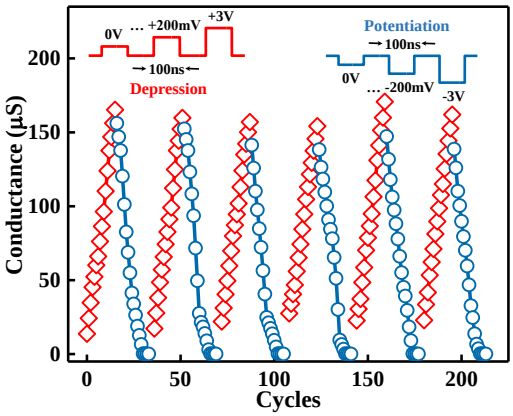

Fig. 4 Continuous modulations of conductance upon the repeated and alternated application of pulses. Insert shows the pulse shape of potentiation: 0V~-3V, depression: 0V~3V.

nm-thick NEI FeFET for its two polarization states, achieved with 10 ns program/erase gate voltage pulses. V_{TH} is defined as V_{GS} at 10^{-7} A·W/L and memory window (MW) is defined as the change in V_{TH}. The NEI Fe FET achieves an MW of 0.9 V with ± 3 V/100 ns program (erase) pulses. Fig. 2(b) benchmarks the NEI FeFET memory device against reported FeFETs, with regard to MW and operating voltages [7-9]. The NEI FeFET device achieves a sizable (> 0.9 V) MW with lower voltages ($|V_{program}| + |V_{erase}| \sim 6$ V) for the thinnest reported FE thickness of 3.6 nm.

The gradual switching in the ferroelectric nanocrystals, which corresponds to a gradual V_{TH} tuning, can be readily exploited to mimic an analog synaptic device. The measured I_D *vs*. V_G curves for a NEI FeFET shift with a series of negative (positive) voltage pulses for potentiation and depression with pulse t_{pw} of 100 ns and 1 µs, were shown in Fig. 3(a) and (b), respectively. Moreover, a continuous modulation of conductance between the two extreme states with t_{pw} of 100 ns over many consecutive cycles was shown in Fig. 4.

The synaptic weight was defined as the channel conductance. Fig. 5(a) shows how the synaptic weight is updated with varying-amplitude 100 ns PD pulses. Conductance values are collected for V_{DS} = -0.05 V and read gate voltage ($V_{GS,r}$) of -0.25 V. The α_p/α_d are extracted using the method in [2], [10]. α_p/α_d can reach 0.08/0.10 with negligible asymmetry, demonstrating that the NEI Fe FET is an ideal candidate for an analog-style synapse.

To mitigate the impact of device-to-device variability as well as to maximize their online training capability, a special NN architecture was proposed recently for analog synapses [11], in which no explicit conductance reference levels are needed and SBP algorithms are used for training. Based on this design, NN online training emulations (*Monte Carlo* simulations) parameterized by NEI Fe FET synapse is performed in Fig. 5(b). Overall, good learning accuracy (~ 94%) is achieved for a varying-amplitude pulse.

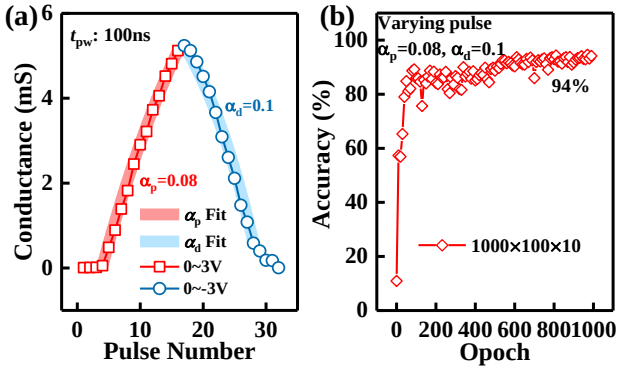

Fig. 5. (a) Demonstration of potentiation and depression of NEI FeFET synaptic weight (conductance) with varying-amplitude 100 ns voltage pulse trains. (b) Simulated CNN's learning accuracy evolution based-on NEI FeFET synaptic behavior. 94% accuracy is achieved using varying-amplitude pulses.

4. Conclusions

We experimentally demonstrate a novel NEI FeFET to be an ideal synaptic device for analog neural network (NN) applications. It achieves a sizable MW with lower voltages compared to previously reported doped HfO_2 based Fe FETs, due to a thinner gate insulator layer. A small α_p/α_d of 0.08/0.10 is achieved with the NEI Fe FET, which is beneficial for analog-style NNs with online training. A CNN is designed and emulated to demonstrate the NEI Fe FET's performance advantages.

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