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Ferroelectric HfO_2 for Memory Applications and Unconventional Computing

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Abstract

Ferroelectricity in hafnium oxide (HfO_2) thin films appears particularly attractive for information storage and might open up a new era of memory devices. Among them, HfO_2–based ferroelectric field-effect transistors (FeFETs) stand out for their low-power field-driven switching, high scaling potential and full CMOS front-end compatibility. Moreover, their peculiar switching properties might be exploited for unconventional applications, such as neuromorphic computing and logic-in-memory concepts. This paper reviews the current status of FeFETs for memory applications and beyond, pointing out the challenges and perspectives.

1. Introduction

Ferroelectric (FE) materials are particularly attractive for storing binary information, due to the presence of two distinct polarization states, which can be switched by an external electric field. Over the past decades, 1T-1C ferroelectric random access memories (FRAM) and 1T ferroelectric field-effect transistors (FeFETs) have emerged as the most promising ferroelectric memory concepts. However, the commonly adopted perovskite ferroelectrics present several shortcomings, such as limited CMOS front-end integration compatibility and poor scalability, which made FRAM commercially viable only for niche applications, whereas the FeFET has never reached the marketplace.

The recent discovery of ferroelectricity in hafnium oxide (HfO_2) promises to solve the abovementioned weaknesses. In particular, the robust and stable ferroelectric properties in ultra-thin layers, with the remanent polarization up to 40 μC/cm^2 and the coercive field $E_C \approx 1$ MV/cm, as well as the full compatibility of HfO_2 to standard fabrication CMOS processes, make currently not only FRAM but also FeFETs promising nonvolatile memory candidates.

This paper surveys the current state of HfO_2–based FeFETs. Main achievements, challenges and perspectives with regard to the memory window, endurance, retention and scaling will be pointed out. Finally, their unconventional applications, such as neuromorphic and logic-in-memory devices will be discussed.

2. Memory characteristics

The FeFET resembles a conventional transistor with the exception of having a FE layer in the gate-stack [1]. The memory effect relies on the two stable polarization states ("up" and "down"), which correspond to two distinct threshold voltage V_T values (high-V_T and low-V_T state, respectively) of the transistor. The operation of setting the device into these states is generally referred to as erase (ERS) and program (PRG) operation, respectively.

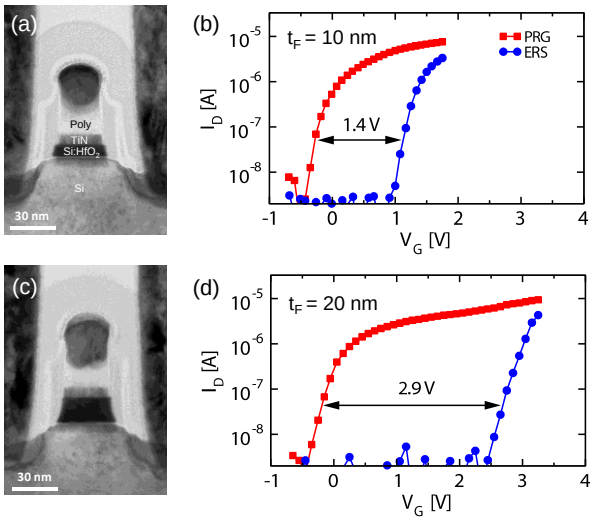

Fig. 1 FeFET memory window for two different FE layer thicknesses (t_F): (a), (c) TEM images of FeFETs with 10 nm and 20 nm thick HfO_2 layer, respectively, fabricated in the 28 nm HKMG technology; (b), (d) the corresponding I_D–V_G curves, respectively.

Memory window

FeFETs having the 10 nm thick HfO_2 (Fig. 1a) typically display a separation between the two V_T states, i.e. memory window (MW), ranging from 1 to 1.5 V [2], as shown in Fig 1b. Moreover, this value might be further reduced under disturbs, which are usually present in memory arrays. To increase the sensing margin and to compete with the mainstream flash memory, strategies to widen the MW are needed. Theoretical considerations suggest increasing the FE layer thickness t_F and/or the coercive field E_C to this aim. However, since E_C is largely invariant in HfO_2 [3], the research has concentrated on the former approach. In fact, it has been shown that by adopting a 20 nm thick HfO_2 layer (Fig. 1c), the MW doubles its value (Fig. 1d). By doing this, the endurance and retention properties are maintained, whereas the switching voltage increases only slightly [4].

Alternatively, it has been reported that a similar MW (≈ 2.8 V) could be achieved by introducing a thin seed layer (ZrO_2) between the FE and substrate [5]. Although this appears attractive, it is not clear whether such a gate-stack composition adversely impacts the switching voltage and the device reliability, and, therefore, necessitates further studies.

A large MW is essential to enable the multi-level operation as well. Reports on single FeFET cells storing more

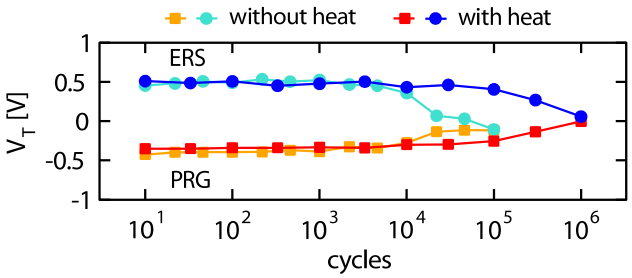

Fig. 2 The switching endurance enhancement with heating pulses.

than two V_T levels testify on the feasibility of this concept [6], [7]. Nevertheless, tight and stable multi-level V_T distributions in large memory arrays are still to be demonstrated.

Endurance and retention

FeFETs in Fig. 1 typically withstand 10^4-10^5 switching cycles, after which the memory window collapses, as shown in Fig. 2. This degradation is attributed to the wear-out of the thin interfacial layer (IL) between HfO_2 and the silicon substrate [8], which is typically made of SiO_2 or SiON. Owing to the large difference in dielectric constant between HfO_2 and IL, a large portion of the applied V_G drops across the IL during PRG/ERS operation. This favors a significant tunneling of electrons during PRG and holes during ERS, whereas the high interfacial field stress induces the generation of defects. Since the created defects act as traps for the injected carriers, the so trapped charge counteracts or even impedes the ferroelectric switching, which finally causes the collapse of the MW as 10^5 cycles are exceeded.

Several strategies for mitigating the field stress on IL have been proposed. These include the operation in the sub-loop regime or the tailoring of the capacitive divider in the gate-stack (e.g. changing the ratio of the areas and/or of the dielectric constants between FE and IL) [9]. Recently, an alternative method of endurance enhancement has been demonstrated, which consisted in applying short heating pulses [10]. In fact, the local Joule heating could recover the created damage within the IL and, thus, extend the cycling endurance for more than a factor of 10, as depicted in Fig. 2. Another approach that might show promise is the high-pressure hydrogen annealing of the IL, which is reported to improve the quality of the IL by passivating the trap sites in metal-ferroelectric-insulator-semiconductor structures [11].

The retention properties of HfO_2−based FeFETs prove to be better than those of the perovskite−based FeFETs. This is explained by a higher E_C in HfO_2 and lower depolarization field E_{dep}, the latter one being mainly due to a lower dielectric constant of HfO_2 with respect to perovskite films. Indeed, two distinct V_T distributions in 64 kbit FeFET arrays could be retained even at 300°C for more than 7 days [12].

Scaling and 3D FeFETs

FeFETs could prove their exceptional memory characteristics even at ultra-scaled technology nodes: at W/L = 80 nm/30 nm in the bulk HKMG technology [2], and W/L = 80 nm/20 nm in the FDSOI technology [12], where W and L are the channel width and length, respectively. Nevertheless, such an aggressive scaling increases the impact of the statistical variations, largely originating from the polycrystalline nature of the FE film. To reduce this impact, a vertical integration of 3D FeFET devices could be a solution. In this way, the device area may not be excessively shrunk, while still maintaining a high bit density. The conformal ALD deposition of the FE HfO_2 has newly enabled the successful demonstration of vertical FeFETs [13], which have the additional potential of re-using of the existing 3D NAND infrastructures developed for flash technologies.

3. Unconventional applications

Large-area FeFETs, which possess a multitude of ferroelectric domains, exhibit gradual switching of the polarization. It is therefore possible to gradually tune the channel conductivity under various pulsing schemes. This property has been exploited in artificial synapses for neural networks [14]. Unlike many other emerging memory based synapses, both potentiation (PRG) and depression (ERS) of the synaptic weights can be made gradual in FeFETs.

Furthermore, FeFETs undergo a complete switching under a train of pulses, even if each of them is insufficient for switching. This accumulative property has been used to emulate the integrate-and-fire artificial neurons [15], which have the potential to largely reduce the size of the existing CMOS neuron circuits as well as to increase their efficiency.

Finally, FeFETs can combine their storage and logic properties to build normally-off logic gates. Indeed, fundamental logic gates, like AND, OR and XOR, have been demonstrated with HfO_2-based FeFETs [16], which operate with a much lower number of transistors compared to the pure CMOS implementations. This sets the basis for more complex logic structures, such as image filters and adders.

4. Conclusions

Ferroelectric HfO_2 might provide unprecedented possibilities for the new era of ferroelectric devices. By leveraging its unique properties, it will be possible to achieve devices both for nonvolatile memories as well as for future computing hardware.

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