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ZrO_2 Anti-Ferroelectric Field Effect Transistor for Non-volatile Memory and Analog Synapse Applications

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Abstract

Anti-ferroelectric field-effect transistor (AFEFET) has been experimentally demonstrated with p-type Ge channels and ZrO_2 gate dielectric (with its thinness down to 2.5 nm). Thanks to the moderate P_r in AFE materials and high-quality ZrO_2/Ge interface, up to 10^6 endurance cycles, and 10 ns program/erase speed are achieved, suggesting a promising candidate for embedded non-volatile memories. Besides, fabricated devices show synaptic behaviors with dynamic (weight tuning) range over 2 orders.

1. Introduction

Doped HfO_2 ferroelectric (FE) materials have attracted extensive interests for embedded non-volatile memory (NVM) applications[1]-[4]. However, challenges exist in several aspects: (1) poor HfO_x/semiconductor interface quality and non-stoichiometry, leading to reliability issues such as wake-up, imprint, and fatigue effects; (2) relatively high remnant polarization (P_r), causing strong depolarization and thus degradation of memory endurance and retention [5]. Recently, anti-ferroelectric (AFE) ZrO_2 was proposed as an alternative, due to potential higher endurance compared to its FE counterpart [6]. Unlike the hysteresis *P vs. V* loop in FE materials, an ideal AFE material shows a "pinched" hysteresis with zero P_r, explained by *Landau-Ginzburg-Devonshire* (LGD) theory [7], are thus not feasible for NVM applications. In practice, deposited ZrO_2 films usually consist of multi-grain/domain textures; with inversion asymmetry in potential (*e.g.* built-in electric field by metal-semiconductor work function difference), the superposition of different AFE domains shifted by this built-in field can result in overall non-zero P_r, as shown in Fig. 1. In this work, we demonstrate ZrO_2 AFEFETs for NVM and analog synapse applications.

2. Experimental details

As shown in Fig. 2, p-channel AFEFETs were fabricated using a conventional CMOS process, starting with an n-type Ge substrate. The gate stack was formed by depositing a layer of ZrO_2 (for 2.5 nm thinness sample, an insulating Al_2O_3 layer was pre-deposited), followed by the TaN gate deposition. After gate formation, source and drain (S/D) regions were implanted by BF_2^+. Finally, an annealing at 500 °C for 30 s was carried. A cross-sectional schematic of the ZrO_2 AFEFET is shown in Fig. 2(b). Figs. 2(c) and (d)

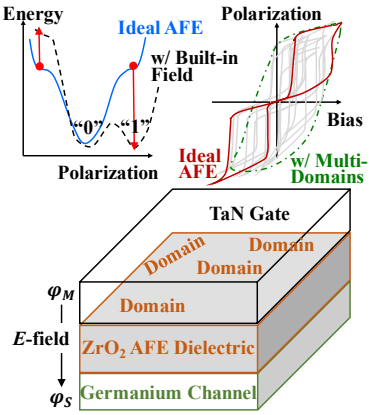

Fig. 1. Illustration of *P-V* curves for AFE materials and AFEFET-based NVM concept.

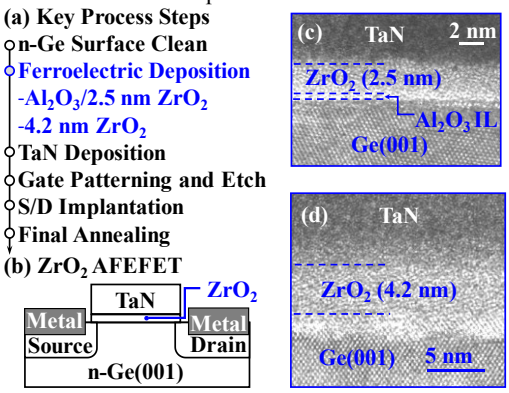

Fig. 2 (a) Key process steps for fabricating AFEFET. (b) Schematic of ZrO_2 AFEFET. HRTEM images showing ZrO_2 thicknesses of (c) 2.5 and (d) 4.2 nm.

show high-resolution TEM (HRTEM) images of ZrO_2 thicknesses of 2.5 and 4.2 nm, respectively.

3. Results and discussions

AFE MOS stacks show hysteresis *P-V* curves with P_r less than 2 (1) μC/cm^2 for 4.2 (2.5) nm-ZrO_2 devices, as shown in Fig. 3 (a). As compared to that of the reported FE devices [1], [2], the smaller P_r value of ZrO_2 AFEFET could potentially improve memory retention and endurance performances owing to the weaker depolarization field. Extracted P_r and critical voltage (V_c) values over 10^6 enduring DC sweeping cycles are shown in Fig. 3 (b), indicating no wake-up, imprint nor fatigue effects, as long-standing issues for FE memories, further manifesting ZrO_2/Ge AFEFET's

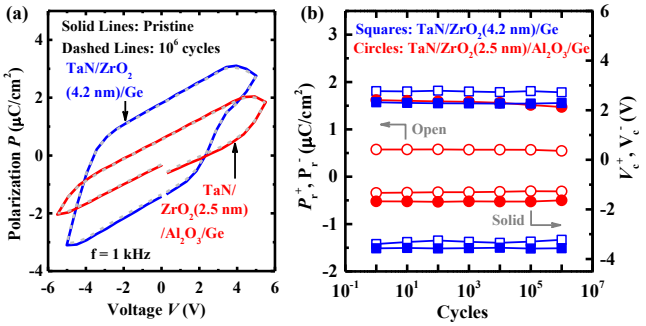

Fig. 3 (a) Measured P-V curves of ZrO_2 MOS capacitors with different ZrO_2 thicknesses during 10^6 sweeping cycles. (b) P_r and V_c *vs.* number of DC sweeping cycles for ZrO_2 capacitors.

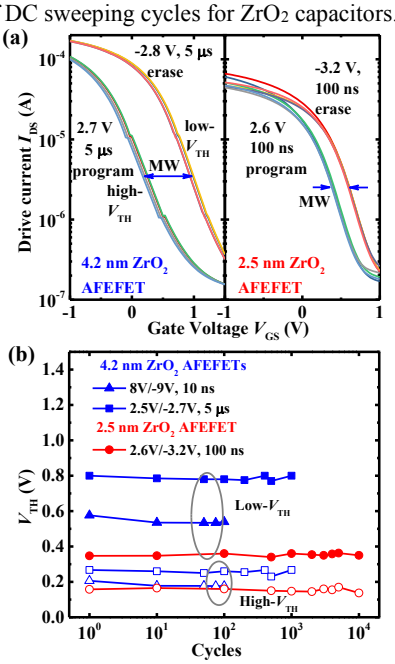

Fig. 4 (a) I_{DS}-V_{GS} curves of AFEFETs for the two polarization states. (b) Endurance measurements under various P/E pulse conditions.

advantages. For NVM applications, the Program (Erase) operation is achieved by applying positive (negative) voltage pulses to the gate of AFEFET, which tends to elevate (lower) its threshold voltage (V_{TH}), and MW is defined as the maximum ΔV_{TH} among the pulse-P/E states, as shown in Fig.4 (a). Fig.4 (b) demonstrates the AFEFET memory endurance tests during pulsed cycles under various P/E pulse conditions, showing the good MW without significant degradation effects. For embedded DRAM replacement, the fastest P/E speed can reach 10 ns in AFEFETs; while for embedded Flash replacement, since P/E speed is relaxed, both lower operating voltage and larger MW are achievable in AFEFETs.

Another emerging application scenario for AFEFETs lies in the computing-in-memory (*e.g.* synapses in neural networks). By taking advantages of the multi-grain/domain nature of ZrO_2 film, the analog-style synaptic behaviors can be demonstrated on AFEFETs. Negative (positive) voltage pulses with gradually increased magnitudes applied on the gate of AFEFETs can be used for potentiation (depression) of the synaptic weights (defined as the channel conductance

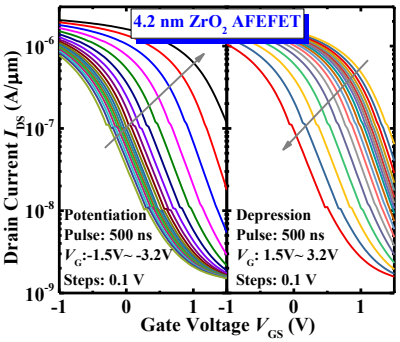

Fig. 5 AFEFET's synaptic behavior: gradual tuning of I_{DS}-V_{GS} curves under pulsed (left) potentiation and (right) depression, starting from high-V_{TH} and low-V_{TH} states, respectively.

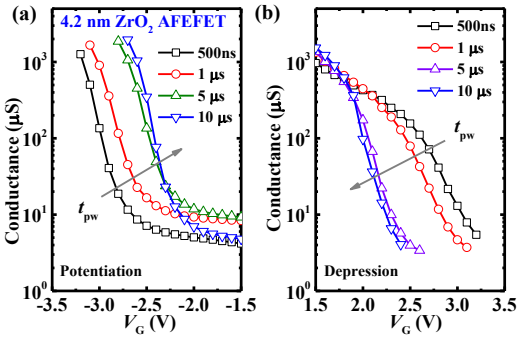

Fig.6 AFEFET channel conductance (read at V_{GS} = -1 V, V_{DS} =-0.05 V) *vs.* write voltages under different pulse widths.

under read conditions). Fig.5 shows measured AFEFET I_{DS} *vs.* V_{GS} curves under a wide range of synaptic operation conditions, suggesting a dynamic range larger than 2 orders, and a tuning "threshold" exists at smaller voltage magnitudes. Extracted weight values are plotted *vs.* tuning voltages under different pulse widths in Fig.6. It is clearly seen that increasing pulse width will generally enhance the weight tuning sensitivity so that a similar dynamic range can be achieved with reduced voltage in synaptic circuits.

4. Conclusions

Due to the reduced P_r and high-quality interface, proposed TaN/ZrO_2/Ge AFEFET structure is an ideal embedded NVM candidate featuring low P/E voltage (dynamic power), high endurance and 10 ns writing speed. Besides, the multi-grain/domain texture of ZrO_2 layer enables analog synaptic operations with large dynamic range, promising for neuromorphic computing circuits.

Acknowledgements

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References

[1] J. Müller et al., IEDM (2013) p.280. [2] M. Trentzsch et al., IEDM (2016) p.294. [3] Q. Luo et al., IEDM (2018) p.47. [4] S. Dünkel et al., IEDM (2017) p.485. [5] M. H. Park et al., MRS Comm. 8, 795, (2018). [6] M. Pešić et al., IEDM (2016) p.298. [7] Landau, L. D. & Lifshitz, E. M. *Electrodynamics of Continuous Media* (1960).