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Design Space Exploration of 1T Non-Volatile Ferroelectric FET Memory for Logic-In-Memory Applications

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Abstract

In this work, the design space of 1T Ferroelectric FET (FeFET) non-volatile memory for logic-in-memory applications has been explored comprehensively considering the impact of ferroelectric parameter variations. NAND/NOR logic functions can be achieved by adjusting the source voltage (V_s) or back-gate voltage (V_{bg}) of 1T FeFET connected in series with a pull-up resistor. The ferroelectric polarization state (FE) and gate voltage (V_g) are the two input of NAND/NOR logic gate. The design space of V_s and V_{bg} for successful NAND/NOR logic functionality has been analyzed quantitatively. Using V_{bg} provides wider design space for successful NAND/NOR logic functions than using V_s. NAND logic function can be achieved by applying positive V_s or negative V_{bg} of FeFET. The comparisons of propagation delay, power-delay product (PDP), and energy-delay product (EDP) of 1T FeFET NAND logic gate with V_s and V_{bg} have been analyzed respectively. Our results show that 1T FeFET NAND logic gate with negative V_{bg} shows 22% improvement in propagation delay, and 22.9% improvement in EDP compared to the 1T FeFET NAND logic gate with positive V_s.

Introduction

Ferroelectric FET (FeFET) with hafnium oxide ferroelectric material has been actively explored for non-volatile memory (NVM) applications due to its high compatibility with CMOS platform [1]. Communication bottleneck between memory and processors becomes one of the most series problems due to low data throughput and high-power consumption. NVM based logic-in-memory circuit has been proposed to alleviate these problems. The reconfigurable NAND/NOR logic gate based on a single FeFET has been presented by applying a specific source voltage or back-gate bias voltage [2]. However, the comparisons between using source voltage (V_s) or back-gate voltage (V_{bg}) of FeFET to achieve NAND/NOR logic functionality have rarely been examined. In this work, the design space, propagation delay, power-delay product, and energy-delay product of 1T FeFET based NAND/NOR logic gate using V_s and V_{bg} have been analyzed comprehensively. Our results show that 1T FeFET non-volatile memory with specific V_{bg} provides better energy efficiency and wider design space for logic-in-memory applications.

Simulation Methodology

Fig. 1(a) shows the schematic of MFMIS FeFET structure used in this work. The ferroelectric (FE) layer thickness (T_{fe}) is 9nm, and the EOT of interfacial layer (T_{IL}) is 0.65nm. In this work, Preisach model is used to characterize the hysteresis of FeFET memory in the TCAD simulations [3]. The extracted coercive electric field E_c = 1.5MV/cm, remnant polarization P_r = 16μC/cm^2, and saturation polarization P_s = 19μC/cm^2 [1] are used in Preisach model. Fig. 1(b) shows the NAND/NOR logic circuit by connecting 1T FeFET with a pull-up resistor in series, and the resistance of the pull-up resistor is 100kΩ. The supply voltage V_{dd} is 1.5V. Mixed-mode transient simulations are performed to analyze the 1T FeFET based NAND/NOR logic functionality in TCAD.

Design Space of V_s and V_{bg} for NAND/NOR Logic Gate

To realize the NAND/NOR logic functionality based on 1T FeFET as shown in Fig. 1(b), the ferroelectric (FE) polarization state and gate voltage (V_g) are the two input and V_{out} is the output of NAND/NOR logic gate. For FeFET with $V_s = V_{bg} = 0$V as shown in Fig. 2(a), at input (A, B) = (FE, V_g) = ("0", "0"), low I_{out} current ("0") is sensed which leads to high V_{out} ("1"). At input (A, B) = (FE, V_g) = ("0", "1") = ("1", "0") = ("1", "1"), high I_{out} current ("1") is sensed which leads to low V_{out} ("0"). The truth table of OR/NOR logic gate is shown in Fig. 2(b). Fig. 3(a) shows that compared to Fig. 2(a), the I_{out}-V_g curves shift to the right by applying positive V_s or negative V_{bg} to FeFET [2]. In Fig. 3(a), at input (A, B) = (FE, V_g) = ("1", "1"), high I_{out} current ("1") is sensed which leads to low V_{out} ("0"); while at input (A, B) = (FE, V_g) = ("0", "1") = ("1", "0") = ("0", "0"), low I_{out} current ("0") is sensed which leads to high V_{out} ("1").The truth table of AND/NAND logic gate is shown in Fig. 3(b). Fig. 4(a) and Fig. 4(b) show the design space of V_s and V_{bg} for achieving successful NAND/NOR logic functionality, respectively. As can be seen, specific V_s or V_{bg} is essential for correct NAND/NOR logic functionality, and using V_{bg} provides wider design window for successful NAND/NOR logic functionality compared to V_s. Table I summarizes the maximum and minimum V_s and V_{bg} for correct NAND/NOR logic functions. The optimal V_s and V_{bg} design have also been proposed in Table I. Fig. 5 shows a successful OR/NOR logic function by using optimal design ($V_s = V_{bg} = 0$V). Fig. 6 and Fig. 7 show that the AND/NAND logic function can be successfully presented by applying optimal V_s or V_{bg} design (i.e. V_s = 0.351V or V_{bg} = -1.742V). Fig. 8 shows that if a large V_s is applied on FeFET ($V_s = 0.52\text{V} > V_{s,MAX}$ shown in Table I), at (FE, V_g) = ("1", "1"), I_{out} is too low which leads to a large V_{out}, and therefore making the logic function fail.

Propagation Delay and Energy Efficiency Comparisons

The optimal design for NOR functionality is FeFET with $V_s = V_{bg} = 0$V. However, the NAND functionality can be achieved by either positive V_s or negative V_{bg}. Fig. 9 compares the energy efficiency of NAND logic gate by applying optimal V_s and V_{bg}, respectively. Optimal V_{bg} design shows 22%, 0.36%, and 22.9% improvements in propagation delay, PDP, and EDP compared to optimal V_s design. This is because raising V_s leads to significant reduction in I_{out} which degrades the propagation delay and EDP.

Impact of FE Parameter Variations on Design Space

Fig. 10 and Fig. 11 show the max/min V_s and V_{bg} design for correct NAND and NOR logic functionality considering the impact of ferroelectric (FE) parameter variations as shown in Table II. Although the max/min V_{bg} design is more sensitive to FE parameter variations, V_{bg} still provides wider design window ($V_{bg,Max} - V_{bg,Min}$) for successful NAND/NOR logic functionality compared to V_s.

In summary, the design space of 1T FeFET based NAND/NOR logic gate has been analyzed quantitively and comprehensively considering the impact of FE parameter variations. Compared to optimal V_s design, optimal V_{bg} design shows better energy efficiency and wider design window for logic-in-memory applications.

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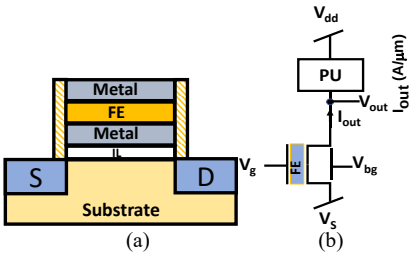
References: [1] V. P.-H. Hu et al., *Symp. of VLSI Tech.*, 2019. [2] E. T. Breter et al., *IEDM*, pp. 669-672, 2017. [3] Sentaurus TCAD, N-2017-9 Manual.



(a) (b)

Fig. 1. (a) Schematic of MFMIS FeFET. (b) 1T FeFET based logic-in-memory circuit by connecting single FeFET with a pull-up (PU) resistor in series. Supply voltage V_{dd} = 1.5V. The resistance of PU is 100 kΩ.

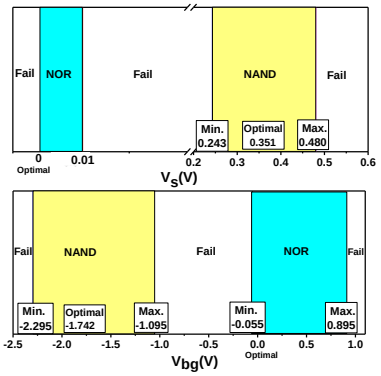


Fig. 4. Design space of V_s (up) and V_{bg} (bottom) for successful NAND/NOR logic functionality. V_s and V_{bg} applied to FeFET within the design window result in correct logic functionality.

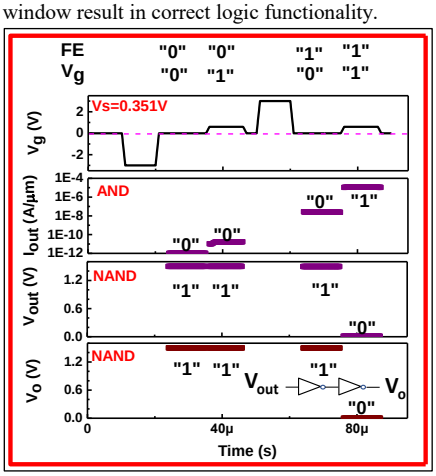


Fig. 6. Transient waveform of correct AND/NAND logic function for FeFET with optimal V_s design (= 0.351V).

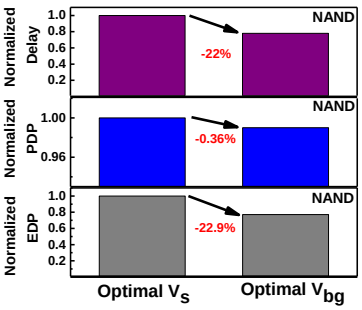
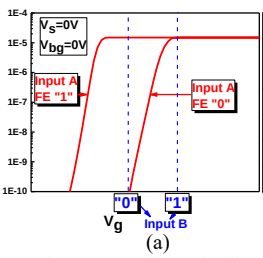


Fig. 9. Propagation delay, power-delay product (PDP), and energy-delay product (EDP) comparisons between NAND logic gate with optimal V_s and V_{bg} designs.



Input A FE	Input B V_g	Output OR I_{out}	Output NOR V_{out}
"0"	"0"	"0"	"1"
"0"	"1"	"1"	"0"
"1"	"0"	"1"	"0"
"1"	"1"	"1"	"0"

(a) (b)

Fig. 2. (a) Schematic illustration of OR/NOR logic gate for FeFET shown in Fig. 1(b) with V_s = V_{bg} = 0V. By applying adequate V_g pulse, the FE polarization can be switch between "0" and "1" states. (b) Truth table of OR/NOR logic functionality. FE polarization state and V_g are the two input of OR/NOR logic gate.

Nominal FE	NOR		NAND	
V_s	Max	0.010V	Max	0.480V
	Min	0V	Min	0.243V
	Optimal	0V	Optimal	0.351V
V_{bg}	Max	0.895V	Max	-1.095V
	Min	-0.055V	Min	-2.295V
	Optimal	0V	Optimal	-1.742V

Table I. The boundary condition of maximum/minimum V_s and V_{bg} to achieve successful NOR/NAND logic functions for FeFET with nominal FE parameters. The optimal V_s and V_{bg} design have also been proposed.

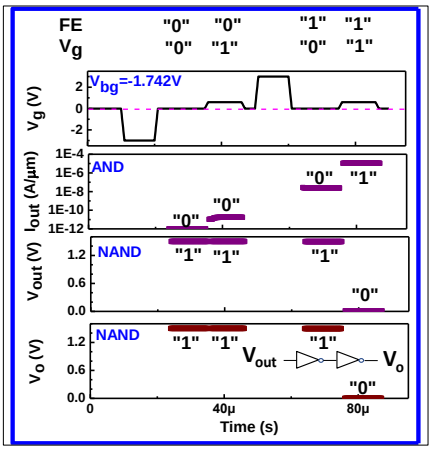


Fig. 7. Transient waveform of correct AND/NAND logic function for FeFET with optimal V_{bg} design (= -1.742V).

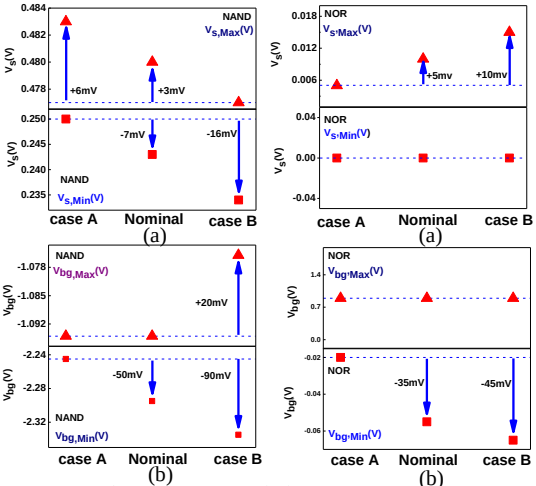
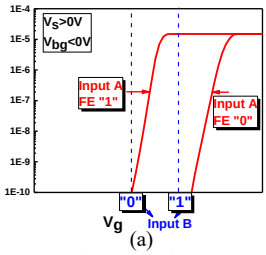


Fig. 10. Impact of FE parameter variations on the design space of (a) V_s and (b) V_{bg} for NAND logic gate. ($V_{s,Max}$ – $V_{s,Min}$) and ($V_{bg,Max}$ – $V_{bg,Min}$) are the design window for correct logic function.

Fig. 11. Impact of FE parameter variations on the design space of (a) V_s and (b) V_{bg} for NOR logic gate.



Input A FE	Input B V_g	Output AND I_{out}	Output NAND V_{out}
"0"	"0"	"0"	"1"
"0"	"1"	"0"	"1"
"1"	"0"	"0"	"1"
"1"	"1"	"1"	"0"

(a) (b)

Fig. 3. (a) The Iout-Vg curves can be shifted to the right by applying positive V_s or negative V_{bg}. (b) Truth table of AND/NAND logic gate.

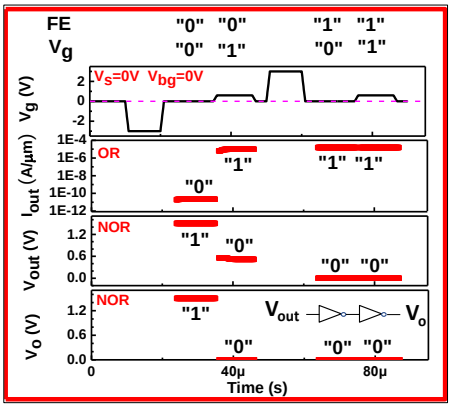


Fig. 5. Transient waveform for successfully realizing OR/NOR logic functionality for FeFET with V_s = V_{bg} = 0V.

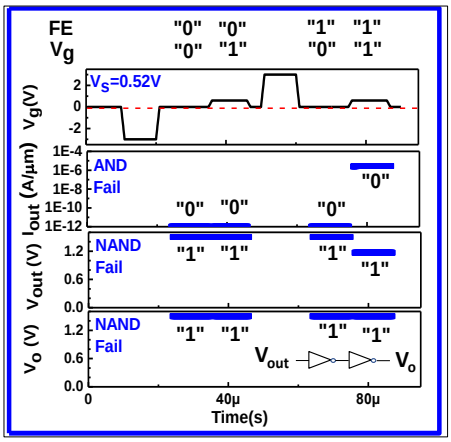


Fig. 8. Transient waveform of AND/NAND logic function for FeFET with large V_s (= 0.52V, larger than maximum V_s shown in Table I). FeFET with too large V_s fail to present the correct logic functionality.

Ferroelectric Parameters	
Nominal	T_{fe} , E_c , P_r , P_s
case A	T_{fe}+3%, E_c+3%, P_r-3%, P_s-3%
case B	T_{fe}-3%, E_c-3%, P_r+3%, P_s+3%

Table II. Nominal FE parameters, case A, and case B used in Fig. 10 and Fig. 11.

With FE variations	NOR		NAND	
V_s	Max	0.005V	Max	0.477V
	Min	0V	Min	0.250V
	(Max-Min)	0.005V	(Max-Min)	0.227V
V_{bg}	Max	0.895V	Max	-1.095V
	Min	-0.020V	Min	-2.245V
	(Max-Min)	0.915V	(Max-Min)	1.15V

Table III. The boundary condition of maximum/minimum V_s and V_{bg} to achieve successful NOR/NAND logic functions for FeFET with ferroelectric parameters variations as shown in Table II.