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Multi-level Operations by Self-clamping Programming Scheme on Fine Floating Gate MTP Cells

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Abstract

A self-clamping programming scheme is proposed for fine floating gate (FG) multiple-time programming (MTP) cells, fully-compatible to standard logic CMOS platforms. Applying this unique feature to multi-level operations is first-time investigated. With especially-designed fine FGs for enhancing the localized charging effect, the new MTP cells exhibit tight threshold voltage distributions through voltage control. In addition, features of improved cycling reliability and fast programming are successfully demonstrated on the new design.

Introduction

As the demand of embedded non-volatile memories (NVM) for numerous integrated circuit systems grows, many logic compatible NVM solutions were proposed and implemented [1]. In our previous work [2], a single poly-silicon floating gates MTP cell on high voltage CMOS platforms was demonstrated. To enhance erase efficiency, an elongated floating gate (FG) was designed to minimize the overlapping area to the erase gate. The long poly-silicon gate is further scaled for enhancing erase efficiency. However, we found that the fine-line FGs are subjected to transient localized charging effect, leading the clamping of the threshold voltage levels during erase operations. In this work, this unique feature is applied to achieve multiple level storage on the MTP cells. Multi-level cells (MLC) [3] are the most effective way to increase data densities and this method has been extended to TLC and QLC technologies in mature flash memories [4]. To prevent overlapping of the states, built-in program-verify loops [5] are incorporated to ensure tight threshold voltage distributions on innumerable cells across a sizable memory array. These complex program cycles not also reduce programming speed, increases power consumptions, but might also leads to long-term reliability challenges [6]. Here, a unique self-clamping scheme on the fine floating gate cells, fully-compatible to standard CMOS process, is investigated for multi-level cell operations with precise V_{th} level control.

Cell Structure and Operation Principles

The proposed MTP cells investigated in this study is fabricated by the $0.18\mu m$ standard CMOS process with single poly-silicon layer. As compared to conventional cells in **Fig. 1(a)**, the new cell (see **Fig. 1(b)**) with an elongated FG narrowed down to less than 160nm is found to exhibit significant localized charging effect. An illustration of the transient response on the fine FG is shown in **Fig. 2(a)**. When a high voltage is applied on the weak control gate (wCG), pulling electrons out through FN-tunneling, the fine poly-silicon prevents charge to reach equilibrium quickly. This leads to positive charging at the tip of the fine poly-Si gate, which, in turn, reduces potential difference between FG and wCG, and breaks FN-tunneling process temporarily. An equivalent circuit model of the fine FG cell is shown in **Fig. 2(b)**, where the high resistance on the fine-elongate sections of the FG can lead to prominent RC delays. As shown in **Fig. 3**, the time-to-erase characteristics of the fine FG cells exhibit unique saturations at each clamping stages. Under high V_{wCG} (Voltage on wCG), **Fig. 4(a)** compares the electron removal rates of the normal and fine FG cells. As a result of the local charging at the FG tip, the FN-tunneling process is interrupted when positive charge is built-up. The simulating potential profile in **Fig. 4(b)** further reveals the effect of local charging on FN-tunneling, which leads to clamping of V_{th} levels. Data in **Fig. 3** suggests that V_{wCG} affects to both the level and time-to-reach each self-clamping stages. The amount of charge being removed before clamping occurs is determined by the speed of charge built-up and the initial FN current level. As summarized in **Fig. 5**, while giving a wider pulse shift the clamping into different phases, the clamped V_{th} levels shift downwards linearly with increasing V_{wCG},. These results suggests that multi-level states can be achieved through V_{wCG} control. The time-to-program from "00" state to the other three state and its corresponding time-to-erase characteristics are summarized in **Fig.6**. Four states at V_{th} of 2.5V、1.5V、0.5V and -0.5V, are obtained by applying different V_{wCG} levels, respectively. Comparing to the conventional program time control MLC operation, see **Fig.7 (a)**, a new voltage level control scheme for reaching precise multi-level V_{th} is proposed, see **Fig. 7(b)**. Through the self-clamping phenomena on the fine FG tips, much tighter threshold voltage distributions can be attained through single pulse programming, where the V_{th} distributions are as compared in **Fig.8**. Operation condition for the fine FG MTP cells are listed in **Table 1**.

Reliability Evaluations

Through the self-clamping programming operation, the fine FG cells not only enables better V_{th} state control, but also induces less cycling damages by preventing overstresses. As compared in **Fig. 9**, the states in normal cells begin to shift considerably after during 1K cycles, while that in the fine FG cells remains stable after 10K cycles. A NOR-type array in **Fig. 10** is proposed to enable program-low, erase-high operations. Program disturb in this array needs to be addressed for cells sharing the same wCG. Disturb characteristic in **Fig. 11** suggests that an inhibit voltage of 3V on sCG can sufficiently prevent the unselected cells from being disturbed. Namely, a maximum number of 1K cells can be placed on a commonly shared wCG. The threshold voltage distributions of 35 cells are monitored before and after the 10 P/E cycling stress. V_{th} distributions on the normal and fine FG cells are compared in **Fig.12**. By the self-clamping MLC scheme, the sensing windows of the fine FG cells can be much tightly controlled as compared to the normal cells, even after 10k P/E cycles.

Conclusion

A new fine floating gate MTP memory on standard logic CMOS platform is demonstrated. With its unique self-clamping operation, the fine FG MTP provide a new approach toward achieving MLC for FG-based logic NVM memory solutions.

References

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[2] Yu-Hung Yeh, et al. SSDM, 2018
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[4] N.Shibata, et al. IEEE JSSC, pp929-937, 2008
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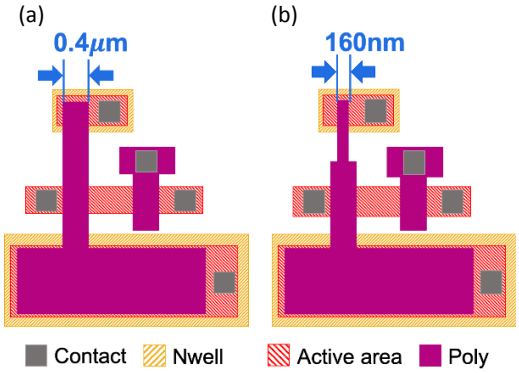

Fig.1 Layouts of the MTP cells (a) with normal FG and that (b) with fine FG, to enhance the localization charging effect.

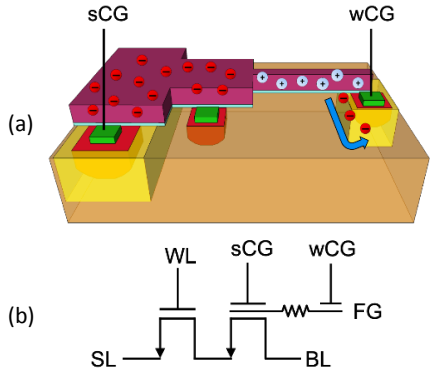

Fig.2 (a) Transient response when electrons are pulled out of a fine FG, local charging occurs at the fine poly-silicon tip. (b) Equivalent circuit model of the fine FG cells.

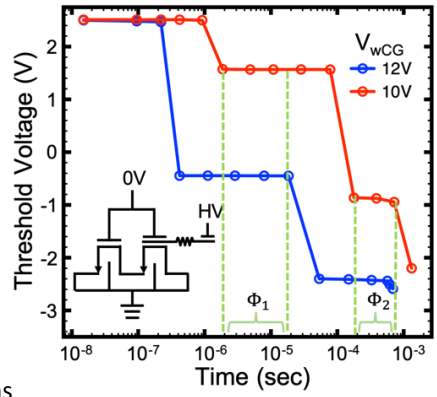

Fig.3 Distinctive states when applying high V_{wCG}, where the clamping effect is caused by the delay in electron redistribution on fine poly-Si lines.

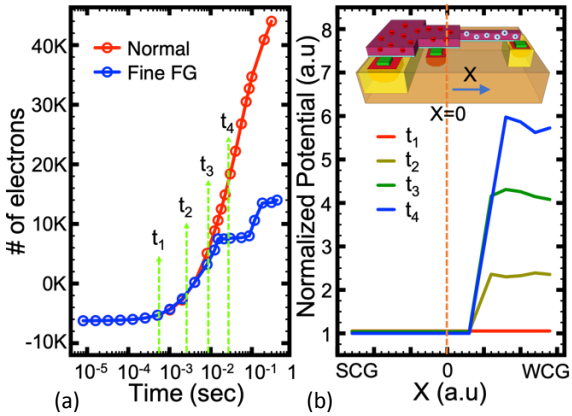

Fig.4 (a) The measured electron removal rates of the two types of MTP devices. (b)Localized charging effect at the fine FG tips shown by the simulated potential profiles.

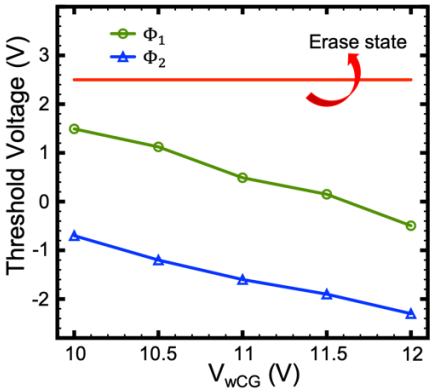

Fig. 5 The clamped Vth levels at both phases (Φ_1, Φ_2 as depicted in Fig.3) depends linearly to V_{wCG}.

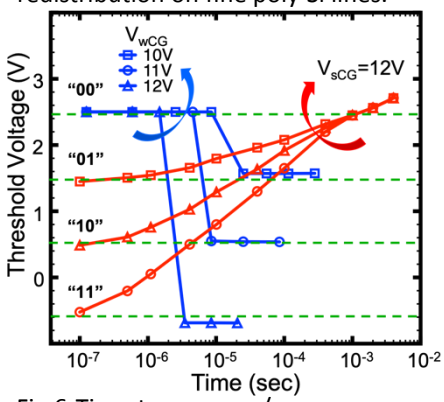

Fig.6 Time-to-program/erase curves for MLC operations obtained by applying continuous pulsing trains.

	Erase	Program		Read
		Select	Unselect	
sCG	12V	0V	3.3V	0V
wCG	0V	10V/11V/12V(10μs)	12V	0V/1V/2V
BL	0V	0V	0V	1.8V
WL	0V	0V	0V	1.8V

Table 1 Summary of bias conditions for MLC operation.

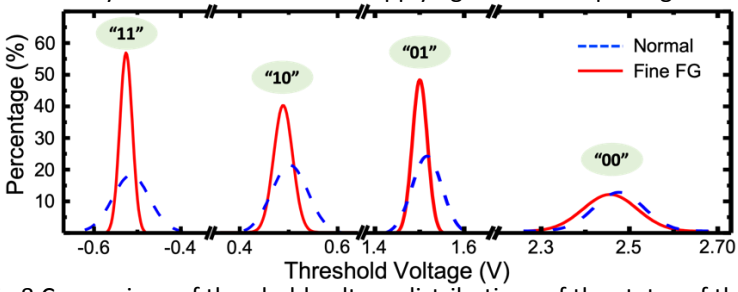

Fig.8 Comparison of threshold voltage distributions of the states of the both types of MTP cells using different single pulse program schemes.

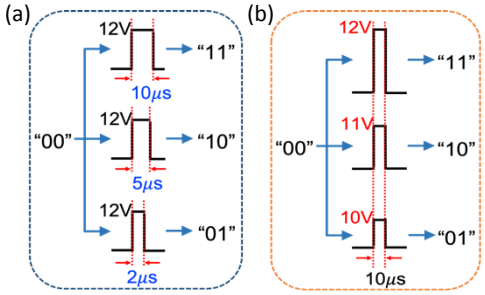

Fig.7 MLC operations for (a) normal devices by pulse width control and that for (b) fine FG cells by voltage magnitude control.

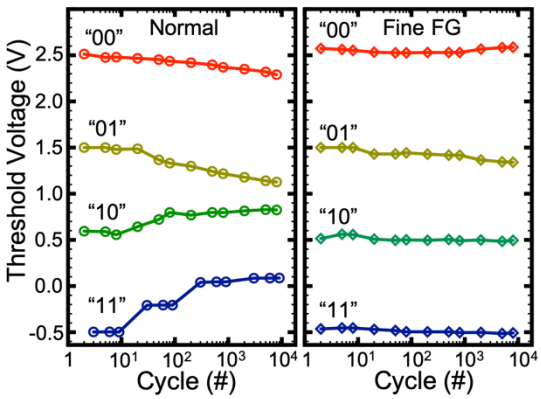

Fig.9 Cycling tests for MLC operation of the normal and fine FG cell. The fine FG cells exhibit higher endurance level in all four states.

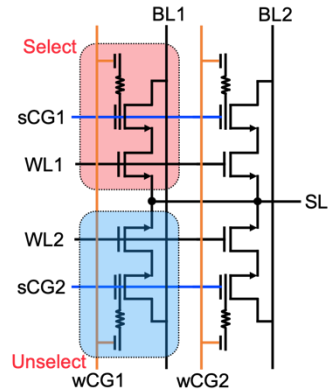

Fig.10 NOR-type array by block erase high and program low operation on selected cells.

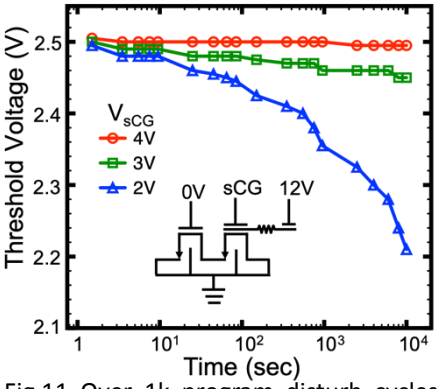

Fig.11 Over 1k program disturb cycles from cells sharing the same wCG can be tolerated when 3V is applied on sCG.

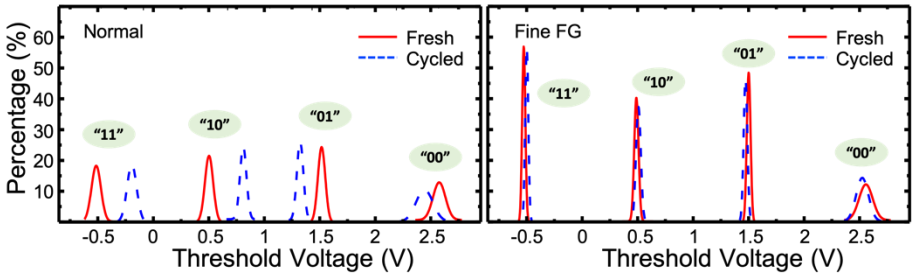

Fig.12 Threshold voltage distributions of normal cells and that of fine FG cells in their 4 states before and after 10K P/E cycling stresses for a sample size of 35 in each group.