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Cross-Coupled Differential Multiple-Time-Programming Memory Cells by CMOS FinFET Technologies

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Abstract

Data retention degradation is one of the key challenges on floating gate based logic non-volatile memories in advanced CMOS technologies. A periodic boosting scheme is proposed for a new cross-coupled differential multiple-time-programming (MTP) memory cell implemented by FinFET CMOS processes. This efficient boosting characteristics enable this solution to be much more competitive in power consumption and scalability.

Introduction

Even with aggressive scaling CMOS technology nodes in the past decade for more compact logic circuits, the cell size for floating gate (FG) based logic non-volatile memories (NVM) remains relatively unchanged [1]. Through more complex cells structure and operation schemes, one hopes to maintain full-compatibility and the performance level of these NVM cells as logic technology scales [2]. The main challenges for these logic NVMs which lie on thin gate dielectric layer cannot contain the stored charge inside the FG for long, leading to data lost problem [3-5]. To solve this problem, in our previous work, a differential FG multiple time programming memory cell has been demonstrated by the CMOS FinFET technology [6]. For data restoration, however, there are significant deficiencies in the proposed the self-boosting scheme [7]. In this work, a new different MTP cells on the same FinFET platform with cross-coupled differential structure is designed to improve the efficiency and reduce the complexity of the period self-boosting operations. In the meantime, large differential sensing window and high endurance of the new MTP cells maintain unaltered.

Cell Structure and Operation Principles

Charge-loss can cause significant data retention challenges when the floating gate is isolated from the channel by the thin gate dielectric layer in FinFET technologies. As shown in **Figure 1**, significant threshold voltage window closure is observed on these cells under bake tests. One of the scheme introduced to extend the lifetime of the storage data is through blanket boosting which restored charge to its initial level periodically. The basic programming mechanism of channel hot electron (CHE) injection on n-channel FinFET is explained in the TEM picture in **Figure 2(a)**. The 2-step blanket boosting scheme proposed to restore the original sensing windows for the original n-channel different MTP is illustrated in **Figure 2(b)**. In addition to the complexity of the blanket boosting operation, the time and power of this boosting scheme limits its application to small memory arrays. Here, a new cross-coupled structure through contact slots to high aspect ratio metal gates is proposed, as shown **Figure 3**. Two select transistors are controlled by the same word line (WL), bit line (BL) and bit line bar (BLB), respectively, while a common control line (CL) and source line (SL) can be shared by all cells in same block. For differential MTP cell, the cell is defined as in state "1" while electrons is placed on FG1, see **Figure 3**. Otherwise, the cell is in state "0". The laterally coupling structure is implemented by closely placed elongated contact slots surrounding the floating gate and through metal wirings for obtaining cross-coupling to the FG on the other branch, respectively, as illustrated in **Figure 4**.

The program/erase characteristics of the original straight cell and that of the cross cells are compared. As shown in **Figure 5**, with negative control line voltage, V_{CL}=-5V, similar time-to-erase characteristics are found on both types of cells, achieving erase time < 0.4msec. **Figure 6** further compares their time-to-program curves. Through channel hot electron injection, the cross cells exhibit slightly slower programming speed as a result of reduced coupling ratio from the CL. Besides, we compare the read current characteristics of the two types of cells in **Figure 7**. As expected, due the decrease coupling from CL, slightly lower saturation read currents are found in the cross cells. Under read condition at V_{CL}=1.5V/V_{BL}=1V, the read current difference is insignificant. The blanket boosting schemes for the straight and cross cell is explained in **Figure 8(a)**, while the time-to-boost characteristics are compared in **Figure 8(b)**. Data reveals that higher charge restoration efficiency on FG1 can be achieved on the cross cell, meanwhile, the disturb inhibition on FG2 is found to be much more effective. The operation conditions for the new cross-coupled MTP cell are listed and summarized on **Table 1**.

Reliability Evaluations

For endurance evaluation, the threshold voltage of 6 cross cells at the two states are monitored during P/E cycling test, as shown in **Figure 9**. Experimental data reveal that the sensing window remains stable after 100k P/E cycles without significant degradation. **Figure 10** shows the distributions of V_{th} of the cross cells shifted on both FG1 and FG2, before and after the proposed blanket boosting operation is applied, where the sample size is 32. Effective boosting results can be achieved. The comparison of the two self-recovery boosting operations for the straight and cross cells is summarized in **Table 2**. The cross-coupled cells show advantages of compact size, much shorter boosting time, less disturb to the other floating gate in a differential cell and much lower energy required for data restoration. For a bake test of 6 samples at 85ºC in **Figure 11,** the stored data can be maintained with no degradation on its data integrity, when a self-boosting step is applied every 50 hours.

Conclusions

A cross-coupled differential MTP cell, fully compatible to FinFET logic process, is proposed. A more efficient self-recovery operation is introduced to remedy the charge-loss problem on the floating gate based MTP, where stable data restoration by sustaining wide sensing windows is demonstrated.

Acknowledgement

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Reference

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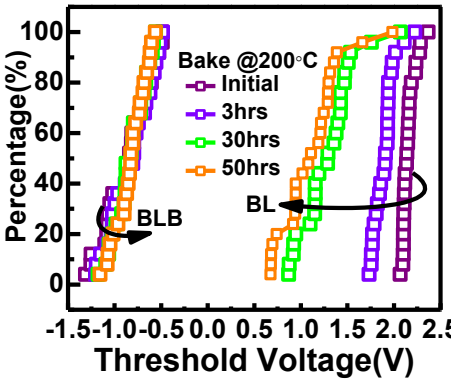

Figure 1 Charge-loss characteristics on the metal floating gate memory cell [3] by FinFET technologies as a result of severe charge lost from the thin gate dielectric layer of less than 5nm.

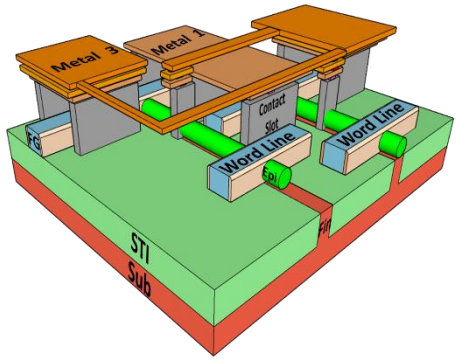

Figure 4 3D illustration of the cross-coupled differential MTP cell with lateral coupling structure to metal floating gates (FG) by twisted wired contact slots.

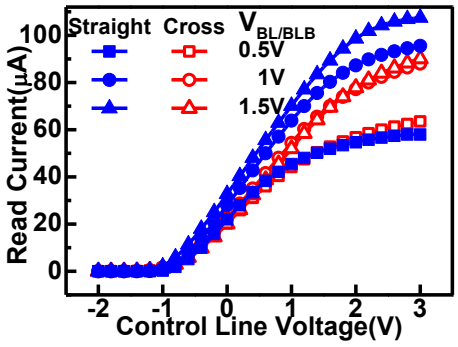

Figure 7 The measured read current characteristics are very similar between the straight and cross-coupled cells.

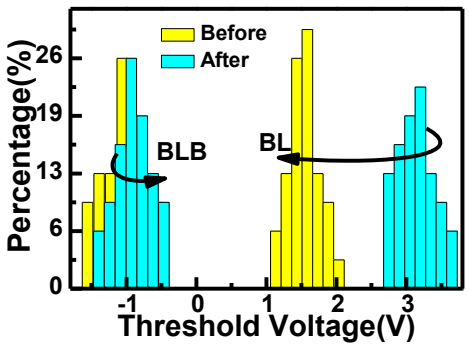

Figure 10 Comparing the threshold voltage distributions of the FinFETs on BL and BLB, respectively, before and after a blanket boosting pulse is applied to all 32 cells under tests equally.

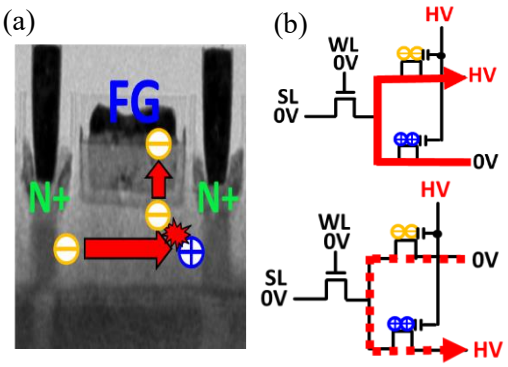

Figure 2 (a) TEM picture of a FG FinFET, with CHE programming operations illustrated. (b) A two-step blanket boosting scheme for n-channel differential MTP cells introduced in [6].

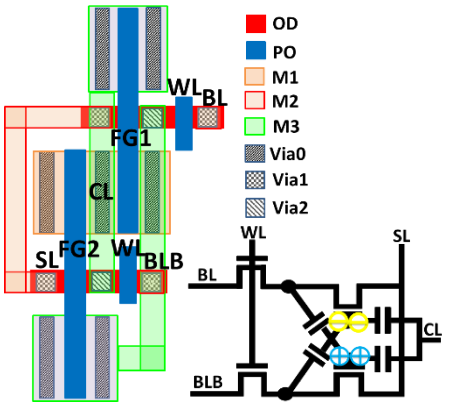

Figure 3 Unit cell layout of the new cross-coupled MTP memory cell and its corresponding circuit schematic.

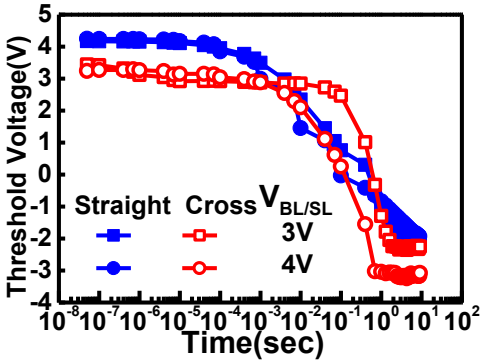

Figure 5 Comparison of the time-to-erase characteristics at V_{CL}=-5V when electrons are pulled out by edge FN tunneling.

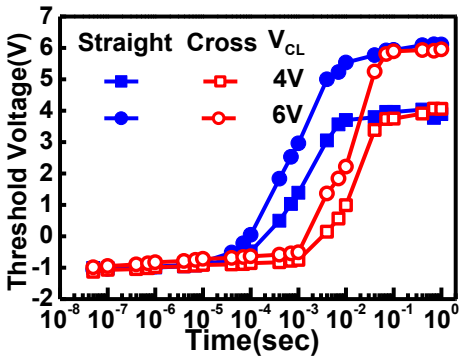

Figure 6 Programming characteristics of two types of cells compared at the same lateral field, where $V_{SL/BL}$=4V.

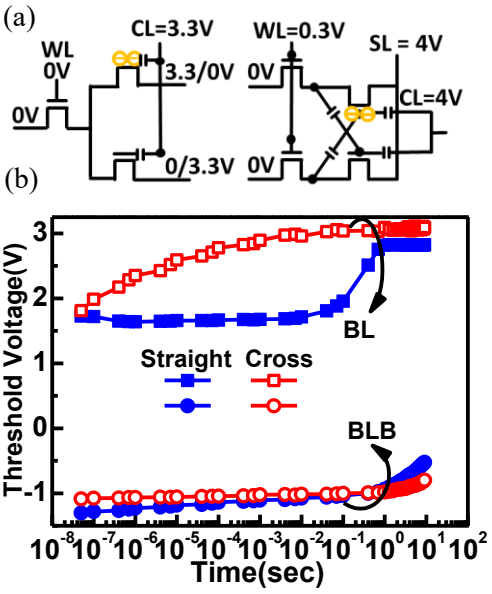

Figure 8 (a) Conditions data restoration for straight and cross cells, respectively. (b) Comparison of the boosting responses.

	Straight	Cross coupled
Area(μm^2)	10.8453	8.6404
PGM/ERS Time(ms)	4/1000	40/0.4
Boost Step(#)	2	1
Boost Time(ms)	1000	4
Inhibit FG Disturb(V)	0.77872	0.2862
Power(μW)	0.83	1.82
Energy(nJ)	581	0.728

Table 2 Features of two self-boosting operation schemes proposed for the straight and cross-coupled MTP cells, respectively.

	WL	CL	BL/BLB	SL
Program	1.8V	4V	0V/4V	4V
Erase	0V	-5V	0V	4V
Read	1.8V	1.5V	1V	0V
Boost	0.3V	4V	0V	4V

Table 1 Operation condition summary.

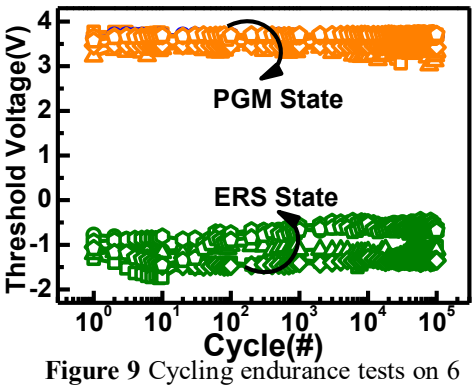

Figure 9 Cycling endurance tests on 6 samples reveal stable V_{th} after 100k.

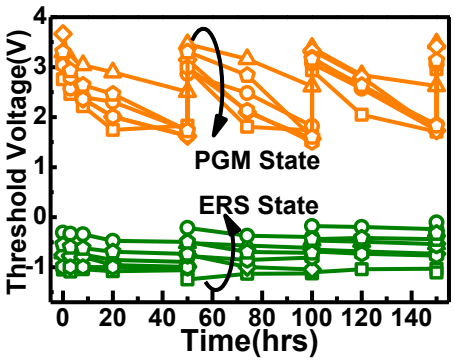

Figure 11 Baked under 85°C, a periodic self-recovery pulse of 4msec is applied every 50 hours to prevent data lost.