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Neuromorphic Technology Using Gated Schottky Diodes with Charge Trap Function

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Abstract

We report a gated Schottky diode (GSD) in which the magnitude of the reverse diode current is the weight of the synapse device. It is a silicon-based synapse device and is fabricated using conventional CMOS technology. Successful vector-by-matrix multiplication is performed on an array of low power GSDs. It is shown that the junction properties of Schottky diodes are highly dependent on sputtering power during metal formation.

1. Introduction

Recent software-based artificial intelligence technologies have shown excellent cognitive abilities. However, it consumes a large amount of power when they are implemented in the von Neumann computing architecture, so research on neuromorphic computing is actively under way. Especially, when using electronic synapse devices, power consumption caused by vector-by-matrix (VMM) multiplication can be drastically reduced. There are many candidates for electronic synapse devices, such as RRAM, PCRAM, and FET-based devices [1]. In this paper, we focus on the gated Schottky diode as a synapse device. It is a silicon based device which can be fabricated with conventional CMOS technology and has the advantage of good reliability. We describe the device characteristics of the fabricated gated Schottky diodes (GSD). Then, a low power VMM is performed in an array composed of these GSDs.

2. Characteristics of gated Schottky diode (GSD)

We fabricated reconfigurable gated Schottky diodes (GSDs) for synapse devices [2]. Fig. 1 (a) and (b) show top SEM view and cross-sectional TEM image of GSD, respectively. S, O, BG_S, and BG_O in Fig. 1 (c) represent the electrodes for the Schottky junction, ohmic junction, and the bottom gates under S and O, respectively. The bottom gates are formed of n^+ doped poly-Si and the active layer is formed of undoped poly-Si. Schottky contacts are formed between Al and unopded poly-Si. The Al is prepared by thermal evaporation. The $SiO_2/Si_3N_4/SiO_2$ stack is formed under undoped poly-Si to store the synaptic weight. Using the bottom gates, the GSD can operate as an *n*- or *p*-type Schottky diode as shown in Fig. 1 (d) and the Schottky barrier height can be modulated. Input bias (V_O) is applied to the O node, and the output current is measured from S node. For example, in the *p*-type GSD, the negative input bias (−2 V) is applied to O node, so the reverse current (I_R) of Schottky diode flowing from S node to O node used as a synaptic current. This synaptic current can be changed by modulating the barrier height.

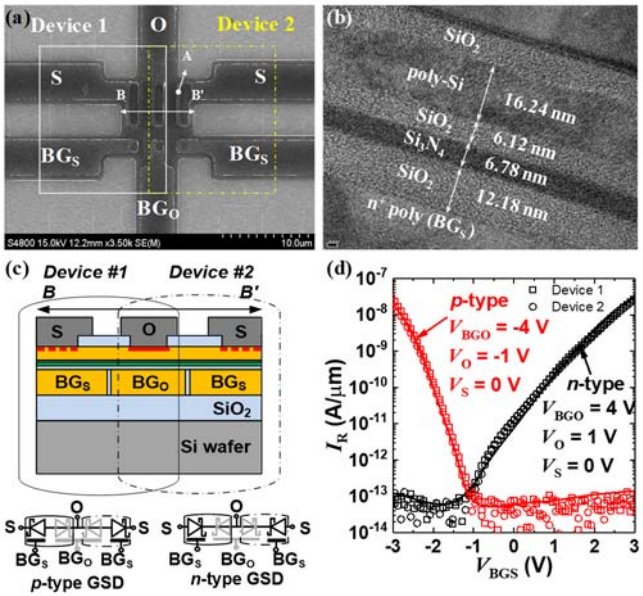

Fig. 1 (a) Top SEM view. (b) Magnified cross-sectional TEM image at point A in (a). (c) Schematic cross-sectional view cut along the solid line B-B' in (a) and equivalent circuit diagram for *n*- and *n*-type GSDs. (d) I_R−V_{BGS} curves of *n*-/*p*-type GSDs measured from one reconfigurable GSD. This figure is reprinted from [2].

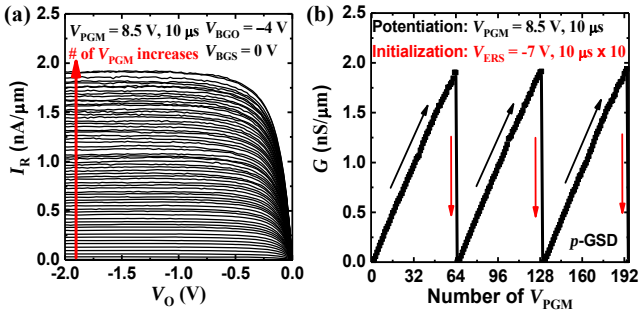

Fig. 2. (a) I_R-V_O curves of a *p*-type GSD obtained by applying pulses for the storage of electrons. (b) Conductance response of a *p*-type GSD. This figure is reprinted from [5].

The input-output characteristic and conductance response of *p*-type GSD are shown in Fig. 2. The synaptic current, which is the reverse current of Schottky diode, saturates with respect to the V_O and this saturation current linearly increases as the number of applied program pulses increases. When the erase

pulse is applied, the saturation current abruptly decreases. The physical mechanism responsible for the property has been described in previous papers [3], [4]. These saturation behavior and linear conductance response of GSD play an important role in hardware-based neural networks. With the help of saturation operation, the synaptic current does not change even when there is noise at the input or output node. In addition, the IR drop occurred along metal wire in an array cannot affect the synaptic current. Through spice simulation, we have successfully verified the inference system of neural networks based on GSDs [6].

3. Gated Schottky diode (GSD) array

The fabricated GSD array was also analyzed [7]. Note the metal for the Schottky diodes in the array is Ti prepared by RF sputtering. A synapse array consists of 10 inputs and 20 output, so the total number of GSD is 200 (Fig. 3 (a)). The synaptic current of a total of 200 devices was measured when V_{BGS} are −4 V, −5 V, and −6 V. The distribution represented by variance (σ) over mean values (μ) of the synaptic current is shown in Fig. 3 (b). Optimization of the fabrication process is needed to reduce the σ. The VMM occupies significant portion of the computational tasks in software-based deep neural networks. However, the sum of the currents of the synapses connected to one column in the synaptic array allows for VMM with very low power consumption. In Fig. 4, the input voltage (−4 V) is applied to ten input nodes (Os) of GSDs to sum the currents flowing through the ten GSDs from one S node. By applying −6 V to the BG_S of ten GSDs, the weights which are represented by the conductance of GSDs are the same. It is confirmed that the sum of the synaptic current of individual synapse devices ($I_1 + I_2 + \ldots + I_{10}$) is almost the same as the I_{tot} measured by applying the input voltage simultaneously to ten synapse devices. Considering the *I-V* characteristics of the GSD, input voltages of various values can be expressed by varying the width of the input voltage pulse having the same magnitude [6]. Then, the weighted sum is expressed as the multiplication of the synaptic current and the time during which synaptic current flows. Since most of synapse devices have nonlinear *I-V* characteristics, this method of using time modulation of voltage pulses can be applied to any synapse devices without error in the VMM operation. As a result, accurate VMM computations can be performed at low power by using our synapse device array. It should be noted that the sputtering power for the Ti formation gives a significant effect on the reverse current property of GSDs. Typical sputtering power for metal wiring is 2 kW, and this power appears to give large damage to the Schottky junction. By reducing the power from 2 kW to 1 kW, the junction property is improved significantly as shown in Fig. 5. In Fig. 5 (b), the reverse current (I_R) is well modulated even if a lower bias is applied to the bottom gate than that in Fig. 5 (a).

4. Conclusions

We have reported the key characteristics of gated Schottky diode (GSD) as a synapse device. The GSDs can be easily fabricated using typical CMOS technology. The GSD operates with reverse diode current, allowing low-power operation. We experimentally demonstrated that accurate VMM is possible in GSD array. The GSD can be a promising candidate for hardware-based neural networks.

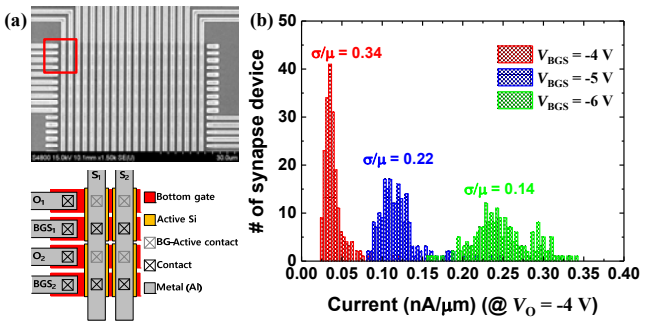

Fig. 3. (a) Fabricated GSD array. (b) Current distribution of the GSD array. Red, blue, and green boxes show three different weight levels represented by I_R when V_{BGS} is −4 V, −5 V, and −6 V, respectively. This figure is reprinted from [7].

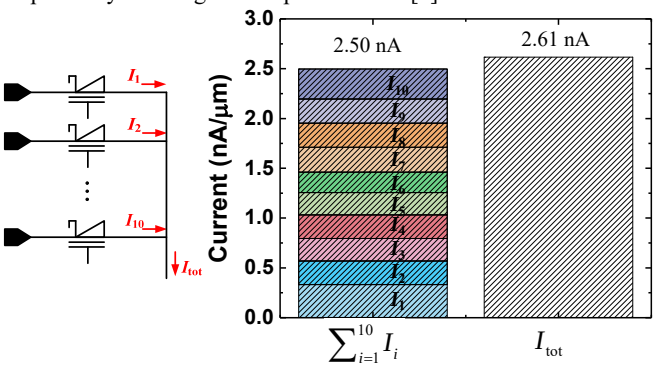

Fig. 4. Vector-by-matrix multiplication (VMM) by using the gated-diode and GSD array. This figure is reprinted from [7].

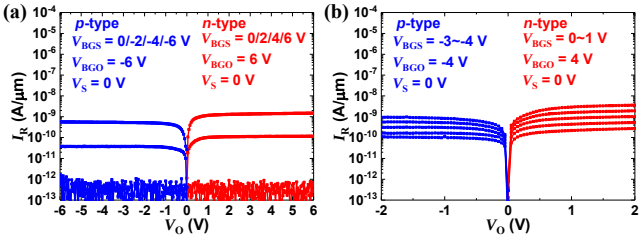

Fig. 5. (a) I_R-V_O characteristics when the sputtering powers are 2 kW and (b) 1 kW.

Acknowledgements

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