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Electromigration scaling limits of copper interconnects

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Abstract

Resistance scaling trends as well as electromigration performance of scaled Cu interconnects will be revised. By using a calibrated physics-based model developed in-house we will explore the electromigration scaling limits for Cu interconnects.

1. Introduction

With the continuous transistor scaling, there is a need to reduce the interconnects size, so that the signals, power and ground can be distributed in the circuit. The increase in Cu line resistance with decreasing area is becoming the limiting factor of the overall circuit performance. One proposal to mitigate this increase in resistance is to replace Cu by other materials (i.e. Co, Ru...) but migrating towards these new metals brings unknown risks during fabrication. The second route is to increase the Cu area in the narrow trench by scaling the barrier and liner (B/L). Besides lowering the resistance, it is of utmost importance that these scaled barriers and liners are continuous enough to allow void free metallization. Also, they need to meet all reliability requirements. In this paper we will give an overview of via and line resistance scaling trends for different metallization options. After that, we will discuss the electromigration (EM) performance of Cu scaled systems on dual damascene structures and finally we will explore the EM scaling limits for Cu interconnects, by using a calibrated physics-based model.

2. Resistance scaling trends

By using the in-house predictive models detailed in [1-3], we are able to benchmark Cu metallizations with TaN and thin self-forming (SF) barriers in combination with Ru and Co liners, as well as Ru and Co metallizations, in terms of line resistance per unit length (R_{Line}) and via resistance (R_{Via}). Fig. 1 shows that Cu resistivity clearly outperforms the Co and Ru metallizations from 40nm down to 10nm for the same metal cross-sections. Nevertheless, when comparing the line resistance and via resistance for the same line and via dimensions and accounting in both cases for the presence of the barrier and liner, we see that at CDs below 22nm alternative metals outperform Cu systems (Fig. 2 and Fig. 3). In order for Cu metallizations to be still used without resistance penalty, it is necessary to reduce the B/L thickness. Fig. 4 shows that TaN/Ru thickness needs to be 0.84nm at 10nm line CD in order to match Ru line resistance.

3. Electromigration

To assess the impact of barrier scaling, failures during electromigration are investigated by testing dual damascene lines with 23nm CD and 22nm vias with AR~2 [4]. The different Cu barrier splits used are detailed in Table I. On split #4, a self-forming barrier is used to ensure the barrier continuity of a possible discontinuous thin TaN barrier. TaN/Co systems show via failures after EM indicating the limitation of this system for further scaling (Fig. 5). TaN/Ru systems are more scalable with failures only occurring in the lines (Fig. 6). Nevertheless, for the same stress conditions, the samples experience a 0.5X decrease in lifetimes with decreasing TaN barrier thickness which could be related to the challenged resistance of the barrier against Cu oxidation and the challenged plating performance on thin barriers (Fig. 7) to guarantee void-free filling. In Fig. 7, we plot also the EM results for 18nm trenches. ~50X degradation on $t_{50\%}$ is observed which is attributed to the decrease of the critical void volume leading to EM failure. ELD Co vias have been proved to have lower resistance than B/L+Cu vias [5] and they are robust against EM (Fig. 8). EM results of a hybrid system (split #5) show similar performance to split #4 and again, no voiding in the via, (Fig. 9), making the hybrid approach a solution for further Cu scaling, considering issues with adhesion and metal intermixing (Fig. 10) are solved [6].

4. EM modeling of Cu scaling limits

By using a physics-based model we are able to investigate the implications of Cu interconnect scaling for electromigration from 90nm down to 10nm [7-9]. This model, calibrated with internal data, allows to assess variations with scaling and impact of metal cap vs. dielectric cap for long lines. Fig. 11 shows a reduction of J_{MAX} falling below 1MA/cm^2 at 22nm CD and below, when using a dielectric cap. It also indicates that, to reach J_{MAX} of ~1MA/cm^2 at 10nm CD Co-cap is essential. For short lines and assuming perfect Flux Divergence Point (FDP), the model predicts an increase on $(jL)_c$ due to the increase of critical stress (Fig. 12). But thin Cu barrier will affect the quality of the Flux Divergence Point. Fig. 13 shows that only 5% leakage through the barrier will reduce the nucleation time of an immortal line leading to failure.

5. Conclusion

The impact of Cu scaling for advance nodes in resistance and electromigration has been discussed and our in-house EM model has been applied to make further predictions. Scaling barrier/liner thickness below 1nm does not show a resistance penalty compared to alternative metals. But EM experiments indicate that reliability requirements will be difficult to reach due to a decrease on lifetime. Experiments also show a ~50X decrease in $t_{50\%}$ for 18nm wide lines (compared with 23nm) which agrees with the J_{MAX} predictions of our EM model. Our models predict that for 10nm wide lines, a Co cap is essential to reach 1MA/cm^2 and, that with a non-perfect FDP the immortal aspect on short Cu lines will be lost.

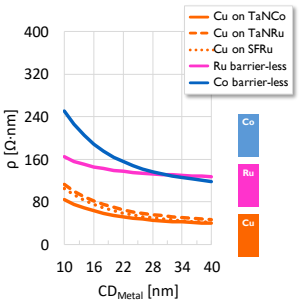

Fig. 1: Resistivity as a function of metal CD excluding the barrier and liner (AR=2) for Cu, Ru and Co fills.

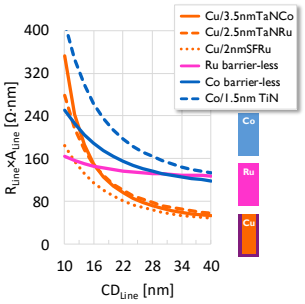

Fig. 2: Normalized R_{Line} as a function of line CD including the barrier and liner (AR=2) for Cu, Ru and Co fills.

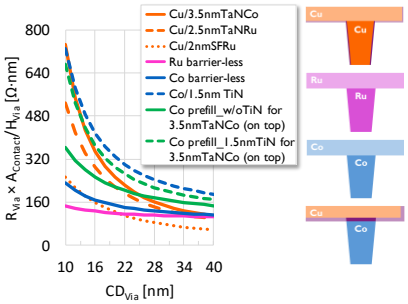

Fig. 3: Normalized R_{Via} as a function of via CD (AR=2) for Cu, Ru and Co fills and Co via-prefill.

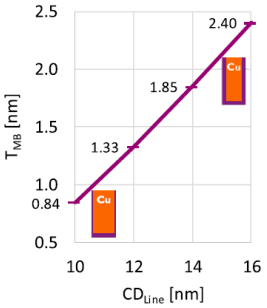

Fig. 4: Equivalent TaN/Ru thickness for Cu to match barrierless Ru line resistance below 16nm half-pitch, when fixing bottom barrier thickness to 2.5nm.

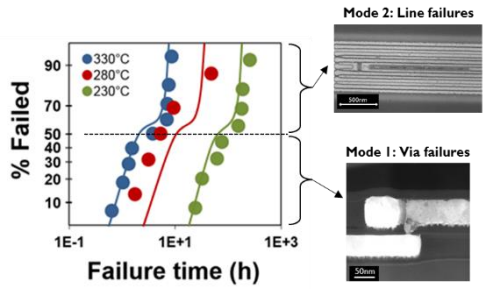

Fig. 5: Samples from 3nm TaN/1nm Co show a bimodal behavior with early and late failures that was correlated to via and line voiding respectively.

TABLE I: M2 METALLIZATION SPLITS USED FOR EM.

Splits	*Barrier*	*Liner*	*Via*
#1	3nm TaN	1nm Co	Cu
#2	3nm TaN	1nm Ru	Cu
#3	2nm TaN	1nm Ru	Cu
#4	1.5nm TaN + 1nm Mn-based	1nm Ru	Cu
#5	1.5nm TaN + 1nm Mn-based	1nm Ru	ELD Co

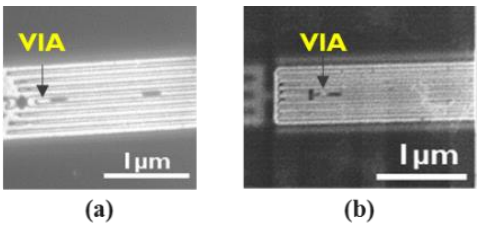

Fig. 6: SEM inspection after EM stress show voids along the line for (a) split #2 and (b) split #3.

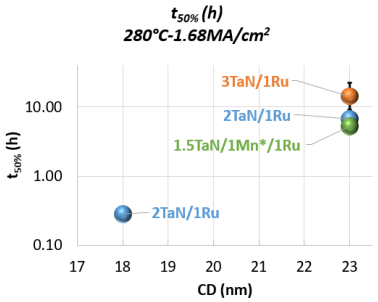

Fig. 7: Impact of Failure time of 23nm lines filled with TaN/Ru/Cu metallization.

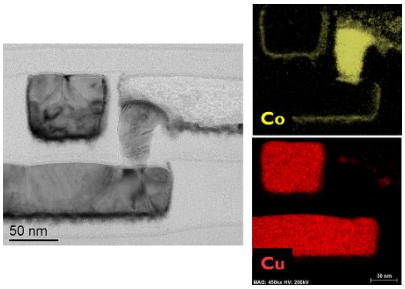

Fig. 8: TEM/EDS of line after EM stress showing voiding along M2 line and Co via intact.

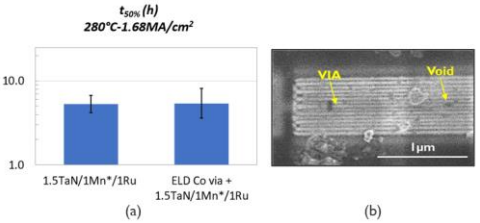

Fig. 9: (a) Similar EM performance of splits #4 and #5 (b) SEM image of line voiding for the hybrid scheme (split #5).

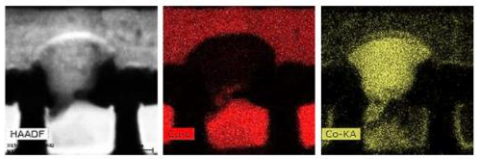

Fig. 10: TEM and EDS of via with high resistance increase after thermal storage for >2600h showing intermixing of Co and Cu and via-sidewall voiding.

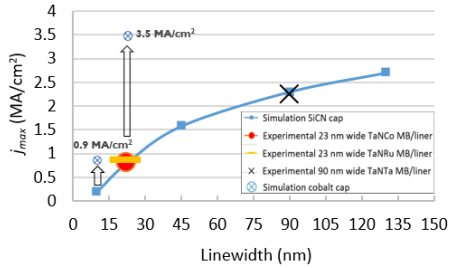

Fig. 11: Impact of scaling on J_{MAX} assessed for long lines.

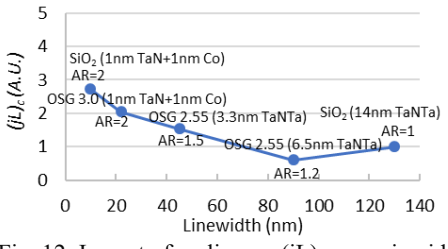

Fig. 12: Impact of scaling on $(jL)_c$ assuming ideal barrier

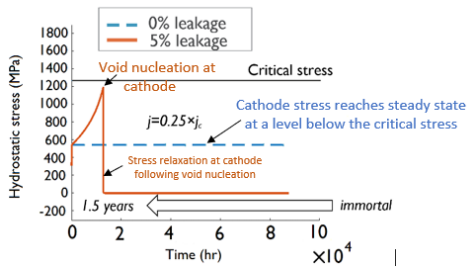

Fig. 13: Impact of flux leakage at the anode on the stress evolution in cathode for 10nm line width.

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