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High Aspect Ratio TSV Formation by Using Low-Cost, Electroless-Ni as Barrier and Seed Layers for 3D-LSI Integration and Packaging Applications

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Abstract

A feasibility study has been carried out for replacing the laborious cum expensive PVD/ALD barrier and seed metal layers by low-cost, highly scalable, CMOS compatible electroless (EL) plated Ni as barrier cum seed layers for the fabrication of sub-micron- as well as 10 μm-width Cu-TSV. Micro-structural data revealed that both sub-micron and 10 μm-width TSVs were completely filled with Cu by using EL-Ni as seed layer. Further, both SEM and EDX results confirms the conformal formation of EL-Ni all through TSV sidewall and TSV bottom, which is otherwise difficult to realize by the even sophisticated PVD tool.

Keywords: Electroless plating, Ni Barrier/Seed layer, sub-micron TSV, Interposer TSV.

1. Introduction

With the advent of TSV (Through Silicon Via) technology [1], an enormous enhancement of computing performance at the edge terminal is being made possible owing to the several order increase in the number of I/Os with smaller form-factor and reduced wire-length. The demand for TSV product is ever increasing since TSV is used for both LSI-integration as well packaging purposes (fig. 1), it is immense to enhance the throughput of TSV fabrication in a less expensive manner. In general TSV fabrication involves the formation of barrier and seed layers (BSLs) deposition by using sophisticated cum laborious PVD, CVD or ALD. Both CVD/ALD relatively form conformal growth. But ALD tool is not only very expensive and laborious, but it involves also higher temperature and slower growth rate. In the case of PVD in spite of its expensiveness, it is hard to realize conformal deposition of BSLs. As shown in fig. 1, the pressing issue is the conformal deposition of BSLs in high aspect ratio (AR) TSV with AR>10, and it is becoming increasing difficult even with ALD.

One way to enhance the throughput for BSLs deposition is electroless (EL) method. Previously for 3D-integration Ni-TSVs were fabricated by EL means [2 & 3], but the AR is ≤ 7. On contrary to PVD/ALD techniques, the advantages of EL method are manifold, such as (1) less expensive in several order, (2) highly scalable (batch process), (3) lower process temperature (around RT), (4) growth is highly conformal (even AR >20), and (5) extremely faster growth rate (μm/min). Recently we have reported the fabrication of Cu-TSV with 10 μm-width and AR 10 using EL-Ni as BSLs [4].

In this work, we report the simultaneous formation of sub-micron as well as microns sized Cu-TSVs using EL-Ni as BSLs respectively for integration and packaging usages..

2. Experimental

A simplified schematic process is shown fig. 2. A test vehicle containing 10x120 μm^2 and 0.8x11μm^2 Si trenches

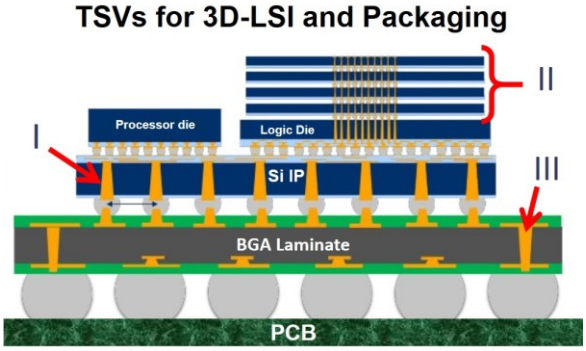

Figure 1. Schematic illustration revealing different types of TSVs namely (I) sub-micron TSVs for 3D-LSI and (II) and (III) fine-pitch interposer TSVs for packaging

with AR ~12 on the same chips were formed on 12"-LSI wafer by Si DRIE, followed by TEOS dielectric deposition via CVD at 300 C. By using the conformal EL-Ni layer inside the TSV, we have carried out Cu-electroplating to fill both the sub-micron as well as microns sized TSVs. Microstructure and conformal EL-Ni formation was checked with SEM and EDX, respectively. Electrical resistivity of the TSVs are measured by I-V measurements.

3. Results and Discussion

Fig. 3 reveals that the sub-micron (800 nm-diameter) patterns transferred into the 12" LSI wafer was intact after hard baking. A meticulous care was taken in order to avoid the pattern collapse during hard baking. Shown in fig.4 is the cross-sectional (X-sec.) SEM images obtained after Si etching using the resist mask of fig. 3. Fig. 4(a) and (b) depict that there exists a severe taper with the tapering angle of 2 deg. at the TSV bottom, which is generally observed for sub-micron sized TSVs with AR > 10.

These trenches were then isolated from the Si by TEOS dielectric deposition followed by EL-Ni plating, and the details regarding the conformal EL-Ni growth inside the high AR TSVs are shown in [4]. Successively Cu-EP was carried out and the field EP-Cu and EL-Ni seed were removed by Cu CMP followed by Ni CMP. Optical images in fig. 5 (a) and (b) for before and after Cu-CMP reveal that these 800 nm TSVs are completely filled with EP-Cu. This confirms the EL-Ni layer well acts as a seed layer for Cu-EPing. Further these EL-Ni is well intact even after CMP, and thus acting as a stopper during Cu-CMP.

Shown in fig. 6 is the X-sec. SEM image for the 10x120 μm^2 Cu-TSVs fabricated by using EL-NI as BSLs. It is clearly evident that the TSVs are completely filled and it is free from voids, which indicates that the conformal growth of Ni was achieved during the EL plating prior to Cu-EPing. It is further evident from the EDX 2D-mapping (fig. 7(a))and energy spectrum (fig. 7(b)) the present of EL-Ni at the outer region of TSVs are conformal, and the TSVs with AR ~ 12 are completely filled with Cu.

In summary, by using conformal EL Ni layers as barrier and seed layers, we have successfully fabricated Cu-TSVs having diameter sub-micron and 10 µm with AR>10, for 3D-LSI integration and 3D-LSI packaging, respectively. Since EL-Ni process is CMOS compatible and extremely low cost compared to PVD or ALD, which confirms that EL-Ni can be potential candidate for 3D-LSI applications.

Ref: [1]A.Klumpp *et al*, ECTC2003 [2]A. Sakuma *et al*, IEEJ Trans. 2009; [3] T. Kawano *et al,* ECTC 2010; [4] M. Murugesan *et al*, ECTC 2019.

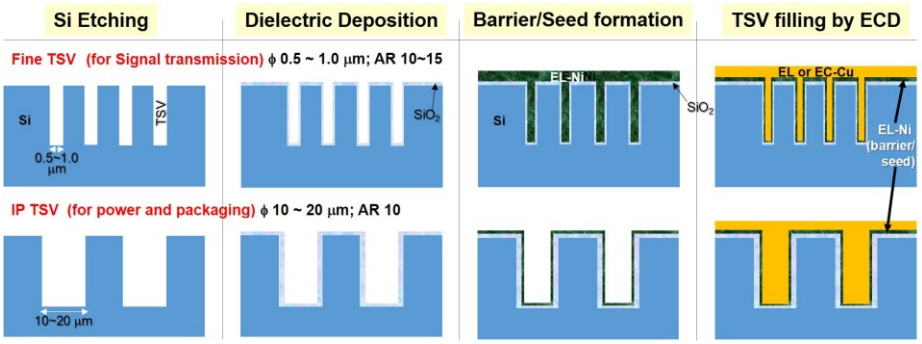

Figure 2. X-sec. schematic view of process flow to obtain the sub-micron TSV as well as an interposer TSV simultaneously by using EL-Ni as barrier and seed layers.

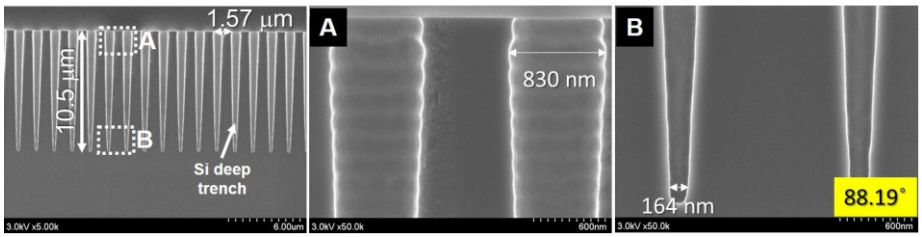

Figure 4. X-sec. SEM images showing the tapered deep trenches formed after the Si DRIE for the sub-micron sized patterns with 0.5 µm-diameter and 1.5 µm-pitch values..

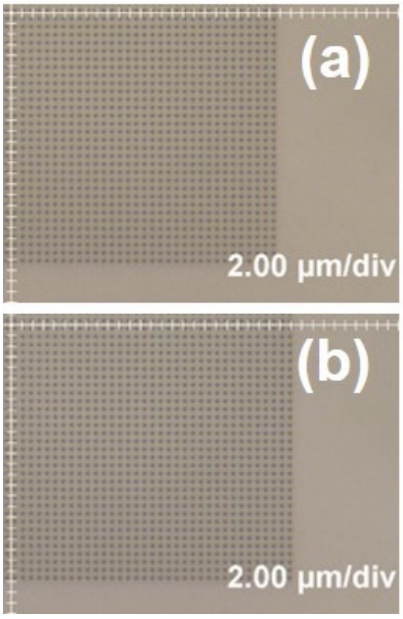

Figure 3. OM images depicting the fine patterns formed by positive tone photoresist, (a) before and (b) after hard baking.

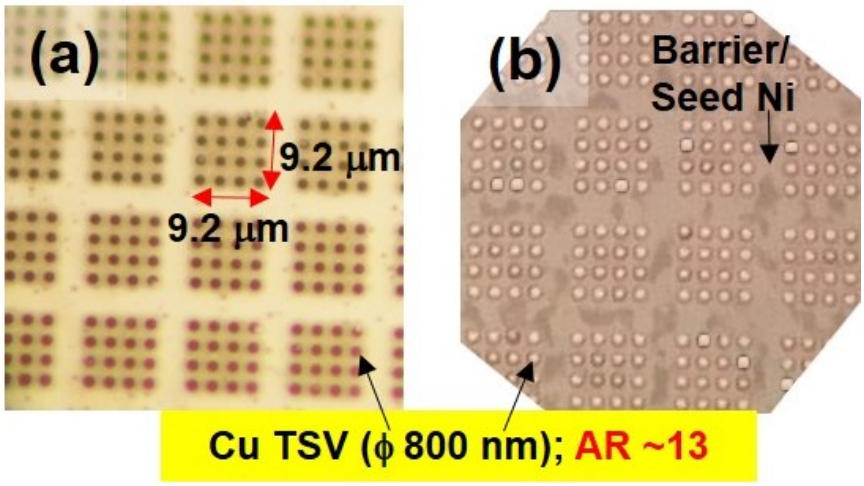

Figure 5. Optical microscopic images revealing the (a) sub-micron Cu-TSVs formed by electroplating of Cu over the EL-Ni as barrier/seed layers and (b) after removing the field Cu formed during TSV filling by Cu-CMP.

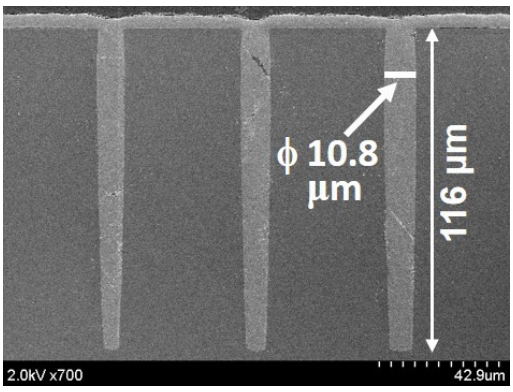

Figure 6. X-sec. SEM image obtained after complete filling of 10 µm-width TSV with AR ~12 by Cu electroplating using EL-Ni barrier/seed layers.

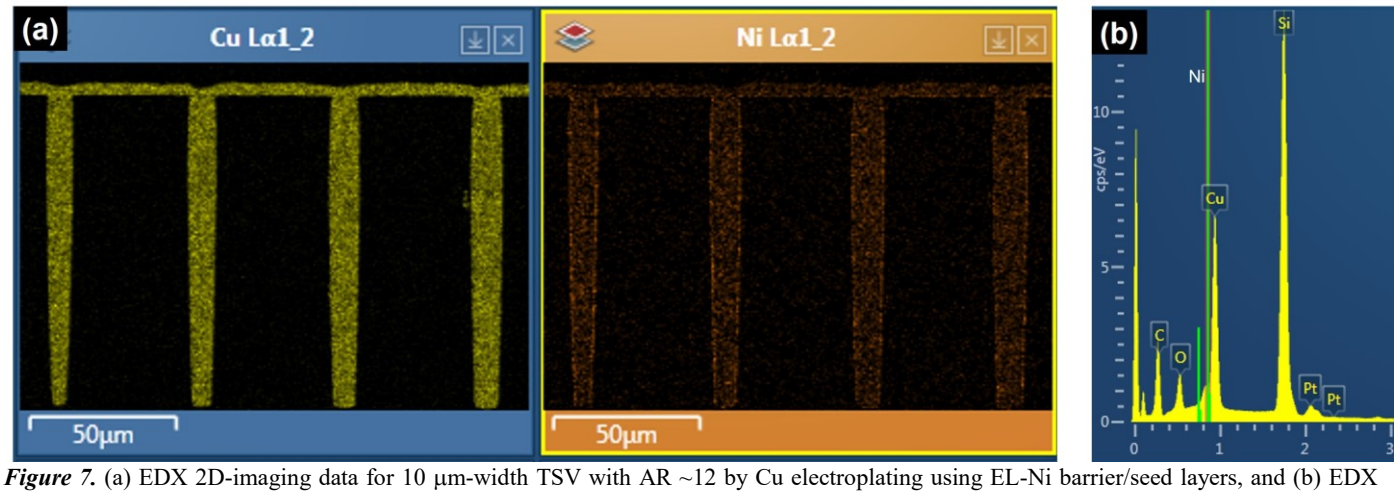

Figure 7. (a) EDX 2D-imaging data for 10 µm-width TSV with AR ~12 by Cu electroplating using EL-Ni barrier/seed layers, and (b) EDX energy spectrum..