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Wafer to Wafer Stacking and Hybrid Bonding for Heterogeneous Integration

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Abstract

3D integration by wafer to wafer stacking is one of the most important technologies for future heterogeneous integration and is a candidate of enabling technology for VLSI scaling beyond 2030. AIST started research and development for wafer-to-wafer stacking and hybrid bonding of 300 mm wafers. In this paper, our new activities are introduced.

1. Introduction

3D integration of electronic devices is an essential technology to enhance functionality and improve performance of electronic systems. Die-to-wafer and wafer-to-wafer stacking are recognized as candidates of 3DVLSI that partitions VLSI at gate or transistor levels. [1] Heterogeneous integration roadmap (HIR) is also discussed by IEEE Electronics Packaging Society (EPS) since 2016. [2] Last year, Intel announced a new 3D packaging technology called “Foveros” that employs die-to-wafer stacking, wafer molding, thinning, TSV reveal and bumping. [3]

We have been researching die stacking with through-silicon via (TSV), nanoparticle deposited fine bumps, and electrical/mechanical/thermal evaluation technologies for 3D integration.

In order to research 3D integration for the next decade, we installed wafer-to-wafer stacking equipment and started research activities of wafer-to-wafer stacking including hybrid bonding of dielectric and metal pad. The equipment is for 300 mm silicon wafers and in operation in Super Clean Room Facility (SCR) of AIST. [4] The new prototype line consists of chemical mechanical planarization (CMP), wafer bonding, wafer thinning, wafer edge trimming, dielectric deposition, i-line lithography with back alignment, Si and SiO_2 etching (deep-RIE), electrodeposition, and some testing and metrology equipment. Existing equipment such as sputtering, annealing, and metal etching are also available.

2. Bonding of Non-patterned Wafers

Process Flow

Figure 1 shows the process flow of water-to-wafer bonding. [5] Wafer surface is polished by CMP and cleaned. Surface roughness should be smaller than 0.5 nm (R_{ms}) to make both surface closer. The surfaces are activated by plasma or fast atom bombardment (FAB). The wafers are megasonic cleaned and spin-dried to remove particles from the surface and adsorb appropriate amount of water molecule on the surface. The wafers are moved to flip station to face the surfaces, roughly aligned at the pre-alignment station. Finally, they are moved to bonding chamber to align bond the wafers. Flip, align and bonding atmosphere can be controlled from atmospheric to vacuum.

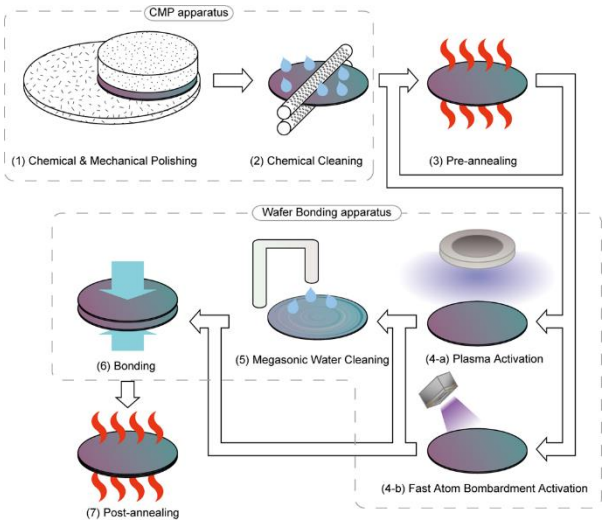


Fig. 1 Process flow of wafer bonding. [5]

Bonding Results of Non-patterned Wafers

Figure 2 shows a scanning acoustic tomography (SAT) image of bonded wafers. The wafer surfaces are activated by plasma and bonded in vacuum. It should be noted that no obvious edge bonding void is observed. This is due to low atmospheric pressure in the bonding chamber. [6]

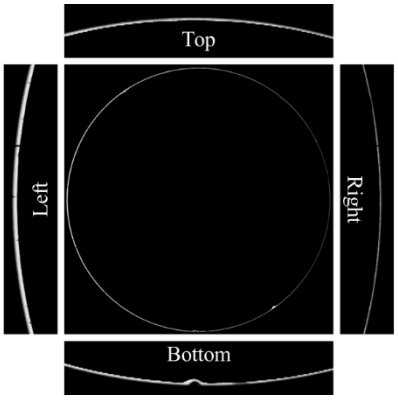


Fig. 2 SAT image of bonded wafers.

The bonding strength measurement by double cantilever beam method [7] showed larger than 1.3 J/m^2 after annealing

at 200 °C for 7 hours in N_2 atmosphere. It is strong enough to endure following processes such as edge trimming, back-grinding and CVD.

2. Bonding of Patterned Wafers

Design of Patterned Wafer

Table I shows the design description of the patterned wafer. Almost all area is covered by bonding pads except scribe lines, alignment marks and verniers.

Table I Design of Patterned Wafer

Item	Description
Die Size	6 mm × 6 mm
Bonding Pad Size	1 μm × 1 μm
Bonding Pad Pitch	2 μm
Bonding Pad Count	~8.8 million/die
Bonding Pad Coverage	~24.5 %
Dielectric Film Thickness	525 nm (TEOS)
Alignment Marks	"Box Brackets" and "Plus Sign"
Other Patterns	Vernier

Process Flow

Figure 3 shows the schematic process flow of patterned wafers.

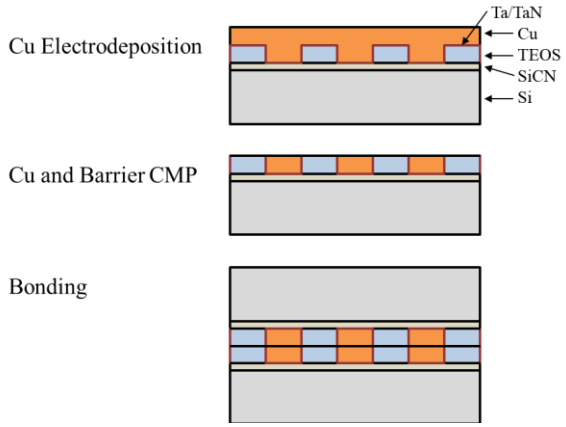
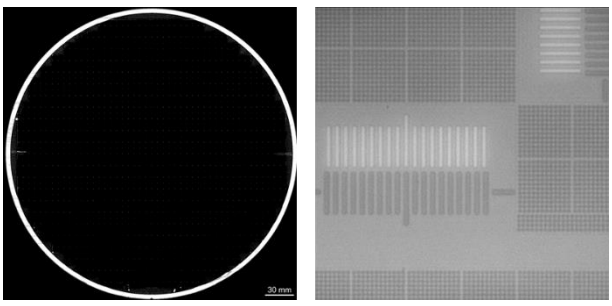


Fig. 3 Bonding Process Flow of Patterned Wafers.

Bonding Results of Patterned Wafers

Figure 4 shows a SAT image of whole wafer (a) and an IR micrograph of and verniers (b).



(a) SAT image of whole wafer (b) IR Micrograph of verniers

Fig. 4 Bonding Results of Patterned Wafers.

There are small pattern dependent voids due to deep dishing of alignment marks and verniers. The dishing depth was more than 20 nm for large "plus sign" pattern of alignment marks. As for small bonding pads, dishing depth or protrusion height were within a couple of nanometers. Figure 5 shows a TEM micrograph of bonded wafers. Bonding accuracy is about 0.4 μm which is not necessarily satisfactory value for logic LSI integration and should be improved.

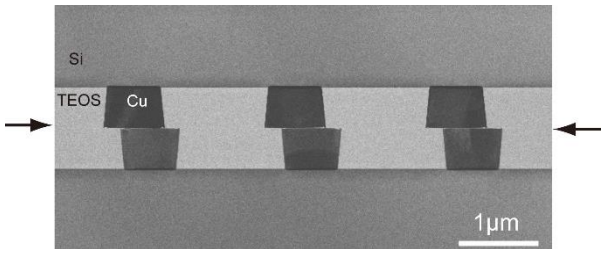


Fig. 5 TEM Micrograph of Bonded Wafers. [5]

3. Conclusions and Future Research

AIST installed wafer-to-wafer stacking equipment and started research of wafer-to-wafer stacking including hybrid bonding. We have confirmed good quality of wafer bonding for non-patterned and patterned wafers.

Wafer bonding of multilevel interconnection wafer with non-patterned wafer, hybrid bonding of multilevel interconnection wafer, and novel analytical methods of bonding interface are the next research theme.

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