

# Development of GaN Power Integrated Circuits

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## Abstract

In this paper, the development of GaN power IC platform will be discussed, on which various peripheral devices can be integrated with power transistors using the same process. Base on the platform, several GaN power ICs will be demonstrated, with focus on a gate driving circuit which exhibits fast switching speed with clean/safe switching waveforms. By incorporating the unique dynamic behaviors of GaN power devices, a new modelling approach for accurate simulation of GaN power ICs will be presented.

## 1. Introduction

Wide-bandgap GaN-based power electronics is a promising solution to high-frequency power switching applications, owing to the superior material properties and the high-speed switching capabilities of the lateral HEMT structure [1]. In the past two decades, effort on GaN power electronics is mainly focused on discrete GaN power transistors, especially the lateral GaN HEMT devices grown on low-cost and highly scalable Si substrate. To fully unlock the potential of GaN HEMT technology, monolithically integrated circuits are highly desirable and have attracted attention worldwide in recent years [2-5]. In this paper, the development of technology platform for GaN power IC platform will be discussed. Our recent effort in the development of GaN power integrated circuits will be presented, with the focus on an integrated gate driving circuit. Modelling of the unique dynamic properties of *p*-GaN gate power HEMTs be discussed for accurate design simulation of GaN power ICs.

## 2. Development of GaN power IC technology

### (1) GaN power IC platform

The lateral nature of GaN heterojunction provides HEMT devices with inherent benefit of high-density integration [5, 6]. To realize cost-effective GaN power ICs, various peripheral devices are required and are preferred to be integrated with power devices at minimum additional cost. A commercial GaN-on-Si power HEMT platform [7, 8] has been shown to be capable of delivering low-voltage E/D-mode HEMTs using the same process as the high-voltage transistors [5]. Field-effect rectifiers can also be implemented by proper reconfiguration of the E-mode transistor structure [9]. 2DEG-channel resistors have been realized for multiple purposes, and high-capacitance-density capacitors have been realized using the *p*-GaN/Al-GaN/GaN stack [10]. Thus, a GaN-on-Si HEMT platform

featuring Schottky-type *p*-GaN gate has exhibited the benefit of multi-functional devices and circuits.

### (2) Integrated GaN gate driver

For high-frequency applications, the parasitic inductances in the gate driving loop significantly degrades the performance of the GaN power circuits, causing ringing effect [11] and false turn-on issues [12]. By integrating the gate driving circuit monolithically with GaN power transistor, the parasitic inductance can be minimized, and fast switching speed with clean/safe switching waveforms can be obtained. Logic controlling circuits have been implemented using E/D-mode transistors, and their capability to operate at ultrafast speed has been verified through a 101-stage ring oscillator, with a propagation delay of  $\sim 0.1$  ns/stage [13]. A charge-pump design is adopted in the bootstrap gate driver to enable rail-to-rail output signal [14]. A GaN power transistor with integrated gate driver was characterized up to 300 V/15 A switching operations using a double pulse tester, and exhibits suppressed gate ringing and fast switching speed. The peak drain voltage slew rate  $dV/dt$  is above 125 V/ns during turn-on, and 336 V/ns during turn-off [14]. In addition, protection function blocks for GaN power ICs has also been demonstrated recently. As an example, an overcurrent protection circuit for GaN power transistor with fast response will be presented [15].

### (3) Modelling for power IC design

To design power ICs, computer-aided simulations are commonly used for concept verification and parameter tuning. The GaN technology is an emerging technology, and device models of the GaN power devices are not well-established. Dispersions are widely observed between dynamic characteristics of GaN power transistors and their static characteristics, including ON-resistance [16, 17], threshold voltage [18, 19], leakage current [20], etc. Among them, the dynamic property of the threshold voltage presents strong impacts on the switching control of the power transistors. Thus, the traditional modelling approaches for silicon power transistors cannot be readily transferred to GaN power electronics. New modelling method has been developed in this work, which incorporates the unique dynamic threshold voltage of GaN transistors, and accurate simulations of the switching characteristics of GaN circuits have been obtained [21].

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## References

- [1] K. J. Chen, et al., *IEEE T-ED*, 64, (3), p. 779, 2017.
- [2] Y. Uemoto, et al., *IEDM*, 2009, p. 165.
- [3] S. Ujita, et al., *ISPSD*, 2014, p. 51.
- [4] D. Kinzer, *ISPSD*, 2017, p. 19.
- [5] C. Tsai, et al., *IEDM*, 2017, p. 737.
- [6] K. Wong, et al., *ISPSD*, 2009, p. 57.
- [7] M. H. Kwan, et al., *IEDM*, 2014, p. 450.
- [8] K. Y. R. Wong, et al., *IEDM*, 2015, p. 229.
- [9] W. Chen, et al., *APL*, 92, (25), p. 253501, 2008.
- [10] G. Tang, et al., *IEEE EDL*, 39, (9), p. 1362, 2018.
- [11] D. Reusch, et al., *IEEE TPEL*, 29, (4), p. 2008, 2014.
- [12] R. Xie, et al., *IEEE TPEL*, 32, (8), p. 6416, 2017.
- [13] G. Tang, et al., *IEEE EDL*, 38, (9), p. 1282, 2017.
- [14] G. Tang, et al., *ISPSD*, 2018, p. 76.
- [15] H. Xu, et al., *ISPSD*, 2019, p. 275.
- [16] M. A. Khan, et al., *Electronics Lett.*, 30, (25), p. 2175, 1994.
- [17] N. Q. Zhang, et al., *IEDM*, 2001, p. 589.
- [18] H. Wang, et al., *IEEE TPEL*, 32, (7), p. 5539, 2017.
- [19] J. Wei, et al., *IEEE EDL*, 40, (4), p. 526, 2019.
- [20] Y. Wang, et al., *IEEE EDL*, 39, (9), p. 1366, 2018.
- [21] R. Xie, et al., *IEEE TPEL*, 34, (4), p. 3711, 2019.