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Demonstration of 1200 V / 1.4 mΩ cm^2 Vertical GaN Planar MOSFET Fabricated by All Ion Implantation Process

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Abstract

In this paper, we present the vertical GaN MOSFET fabricated by all ion implantation process. The fabricated MOSFET shows a breakdown voltage of 1200 V and an effective on-resistance of 1.4 mΩ cm^2. This result will greatly contribute to the realization of GaN power devices.

1. Introduction

From the height of its potential, Gallium nitride (GaN) has attracted attention as a semiconductor material capable of realizing a further low loss power device [1]. Considering the application to a high power switching system, the vertical device structures on GaN bulk substrates (GaN on GaN) and MOS gate driving is preferable from various viewpoints. Due to the progress of bulk GaN crystal growth in recent years [2], reports of vertical type GaN MOSFETs or diodes exceeding breakdown voltage of 1 kV on GaN substrates have been demonstrated so far [3-5]. However, these demonstrated devices utilize the pn junction formed by epitaxially-grown Mg doped layers.

Taking practical use and reliability into consideration, it is essential to form a p-type layer by ion implantation (I/I). However, p-type formation by I/I into GaN is known to be extremely difficult. It is only recently that the possibility of p-GaN formation by Mg I/I have begun to be reported [6-9]. We also reported MOSFET operation formed on the Mg I/I layer and the control of the threshold voltage with Mg dose [10]. In addition, we also reported that the sequential N I/I to Mg I/I layer is effective to improve the breakdown voltage of pn junction [11]. These reports show the possibility of realizing MOSFET devices using p-type I/I. However, there is no report for GaN vertical MOSFET with high breakdown voltage fabricated by all I/I process. In this study, we demonstrate the vertical GaN planar MOSFET with high breakdown voltage and low on-resistance fabricated by all I/I process.

2. Device fabrication

Fig. 1 shows a schematic images of the fabricated vertical GaN planar MOSFETs by all ion implantation process. Firstly, the Mg I/I was carried out selectively on 10-µm-thick n-GaN layers grown by metal organic chemical vapor deposition (MOCVD) on the n-type GaN (0001) substrates obtained by ammonothermal method. The carrier density of n-GaN epitaxial layer is around 1×10^{16} cm^{-3}. The Mg-ions were implanted with 10 to 700 keV and the total dose was set to 6.5×10^{13} cm^{-2}. After Mg I/I, N I/I was carried out sequentially. The N-ions were implanted with 10 to 600 keV and the total dose was set to 6.7×10^{13} cm^{-2}.

Secondly, Si-ions were selectively implanted into the source regions with 15 to 40 keV and the total dose of 1.9×10^{15} cm^{-2}. Thirdly, O-ions were selectively implanted into the JFET region with 10 to 700 keV and the total dose of 2.3×10^{13} cm^{-2} to reduce the JFET resistance.

After triple I/I, the wafers were annealed at 1300 °C in N_2 atmosphere for 5 minutes with AlN encapsulation cap to prevent dissociation of GaN during high temperature annealing. After the annealing, the AlN cap was chemically removed. The typical root-mean-square (RMS) surface roughness of GaN after activation annealing was 0.25 nm, determined by AFM measurement in 1 µm square area.

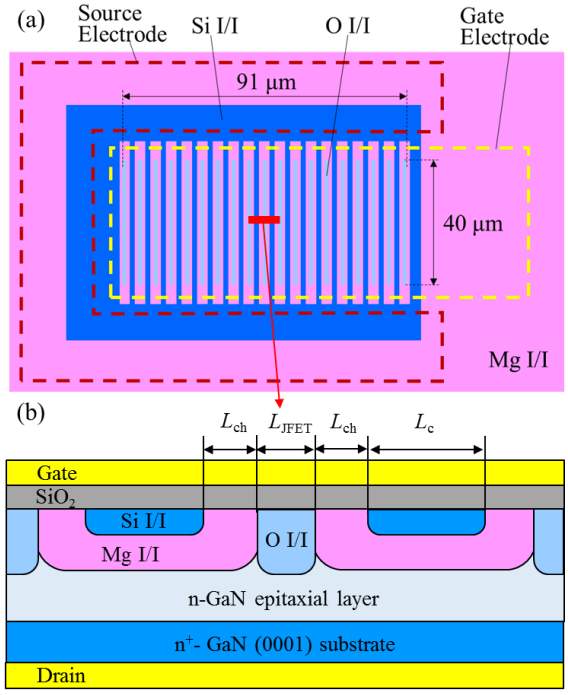

Fig. 1 Schematic images of vertical GaN planar MOSFETs with all ion implantation process. (a) plan view without SiO_2 layer, (b) cross sectional image of active region

100-nm-thick SiO_2 layers were deposited at 300 °C by a plasma-CVD apparatus with TEOS gas. Titanium and Aluminum metal was used as a gate, source and drain metal. The body contact metal was Ni. A forming gas annealing was performed at 400 °C for 30 min.

The layout of the active region was stripes with a cell pitch of 5 μm. The designed size of the active region on photomask was 91 μm and 40 μm. The designed channel length (L_{ch}) was 1 μm. The JFET length (L_{JFET}) was 1 μm and the source length (L_c) was 2 μm. Since the source electrode is in contact with the active region at a position apart in the horizontal direction as shown in fig 1 (a), the source resistance is large as compared with the stacked electrode in vertical contact with the source I/I region.

3. Results and discussion

Fig. 2 and Fig. 3 show the I_d-V_d output characteristics and the I_d-V_g transfer characteristics in the linear region on fabricated GaN MOSFETs, respectively. Fabricated MOSFETs show the normal MOS channel behaviors, such as the good drain current control by the gate voltage, the good ohmic contact and the low gate leakage current (<1.0×10^{-3} A cm^{-2}), and normally-off operation with positive threshold voltage (V_{th}). The V_{th} determined as a gate bias intercept of the linear extrapolation of I_d-V_g curve was 2.45 V. The on-resistance determined from the slope of the I_d-V_d curve at V_g = 30 V and V_d = 1 V was 2.78 mΩ cm^2. In consideration of the current spread in the drift layer, the area of the active region used to calculate the on-resistance was set to 101 μm and 50 μm by adding the drift layer thickness (10 μm) to the designed size of the active region.

From the evaluation of each on-resistance component in the vertical MOSFET, it was confirmed that the source resistance was 1.38 mΩ cm^2, the channel resistance was 0.38 mΩ cm^2, the JFET resistance was 0.21 mΩ cm^2 and the drift resistance was 0.81 mΩ cm^2, respectively. The source resistance can be reduced by using a stacked electrode structure in vertical contact with the source I/I region. Therefore, the effective on-resistance of the active region excluding the source resistance was calculated to be 1.4 mΩ cm^2.

Fig. 4 shows the breakdown measurement of fabricated GaN vertical MOSFET. The breakdown voltage was measured under applying -5 V to the gate electrode. The fabricated GaN vertical MOSFET was broken at about 1200 V. The drain leakage current at 1000V is less than 1.0×10^{-3} A cm^{-2}. Therefore, the vertical GaN planar MOSFET with a breakdown voltage of 1200 V and an effective on-resistance of 1.4 mΩ cm^2 in the active region could be realized by the all ion implantation process.

4. Conclusions

We have demonstrated the vertical GaN planar MOSFET with high breakdown and low on-resistance fabricated by all ion implantation process. These results will greatly contribute to the future development of GaN power devices.

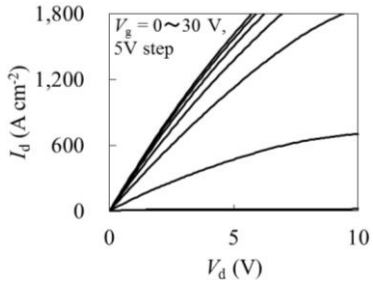

Fig. 2 I_d-V_d output characteristics of fabricated GaN MOSFET

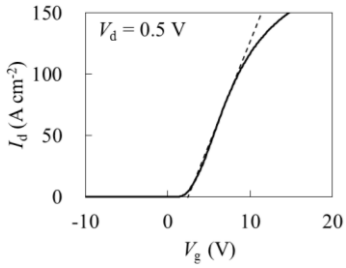

Fig. 3 I_d-V_g transfer characteristics of fabricated GaN MOSFET

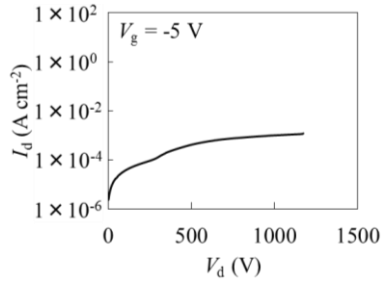

Fig. 4 I_d-V_d breakdown measurement of fabricated GaN MOSFET

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