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Suppression of Short-Channel Effects in Normally-off GaN MOSFETs with Deep Recessed-Gate Structure

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Abstract

We have demonstrated the suppression of short-channel effects in normally-off GaN MOSFETs with deep recessed gate structure. TCAD simulation results show that the electric field concentration is effectively reduced at the recessed edge of the MOSFETs with the deeper recessed gate structure. The MOSFET gate structures with different recess depth ranging from 45 nm to 165 nm were fabricated and evaluated. The experimental results suggest that the deeper recessed-gate structure is effective for suppression of the drain-induced barrier lowering (DIBL) and improvement of subthreshold swing (SS) and threshold voltage roll-off.

1. Introduction

GaN field-effect transistors (FETs) have been studied recently with a view to their application in high-frequency amplifiers and power devices [1]. For the power devices application, normally-off devices are required for fail-safe operations. Although various types of normally-off GaN transistors were proposed such as cascade devices, JFETs, and MOSFETs [2-4], the most preferable device structure to exploit the inherent GaN characteristics is the MOSFET in terms of both cost and device performance. Because MOSFETs can directly control the channel potential with gate-source voltage (V_{GS}), fast-switching operation can be achieved. In normally-off GaN MOSFETs, the recessed-gate structure has been studied by removing the AlGaN barrier layer under the gate [5]. This structure may have the problem of high channel resistance (R_{ch}) because of the low electron mobility in the recessed region. Since the shorter-gate-length (L_g) structure is proposed to reduce the R_{ch}, there is concern regarding the degradation of DIBL and SS and negative V_{th} shift owing to short-channel effects (SCEs). Although double-recess overlapped gate and dual-gate structure were studied [6, 7], issues remain to be solved regarding mass production and cost in view of the complicated fabrication process.

In this work, simple approaches to suppress SCEs by using deep recessed-gate structure are demonstrated.

2. Electric Field Analysis in TCAD Simulation

Firstly, the electric field distribution was calculated in the recessed GaN MOSFETs by means of 2-D device simulation. The simulations for the comparison of SCEs were carried out in AlGaN/GaN HEMT structures with recess depth of d = 45, 120, and 240 nm. The calculated device conditions are L_g = 1 μm, V_{GS} =10 V, and drain-source voltage (V_{DS}) = 10 V. Fig. 1 shows the calculated electric field distribution around the edge of the recessed gates with three different recess depths. The electric fields are concentrated at the edges of the recessed gates. Making the recess depth deeper, it is clearly found that the electric field intensity at the edges of the recessed-gates is reduced. When the recess edge is close to a 2-dimensional electron gas (2DEG) region, the electric field intensity of the recess edge is increased (Fig. 1 (a)). On the other hand, when it is far from a 2DEG (Fig. 1 (b) and (c)), the electric field intensity is decreased.

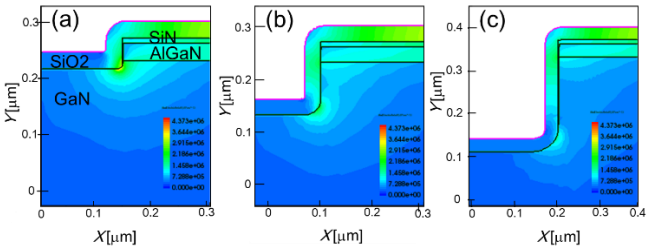

Fig. 1 Electric field distribution for three different recess depth of (a) d = 45 nm, (b) d = 120 nm, and (c) d = 240 nm.

3. Device Structure and Fabrication

To demonstrate the suppression of SCEs, GaN MOSFETs with deep-recessed gate structure were fabricated. The schematic images of the recessed-gate GaN MOSFETs are shown in Fig. 2 with four different recess depths of (a) Ref. (d = 45 nm) and (b) deep-recessed gate structure (d = 105, 125, 165 nm). The fabrication process is as follows. An $Al_{0.2}Ga_{0.8}N$ (30 nm)/GaN/Buffer layer was grown on a Si substrate by the MOCVD method. A SiN surface passivation film was deposited on the AlGaN barrier layer. The recess structures were fabricated by inductively coupled plasma reactive ion etching (ICP-RIE). Here, the recess structure had the four different depths of d = 45, 105, 125 and 165 nm.

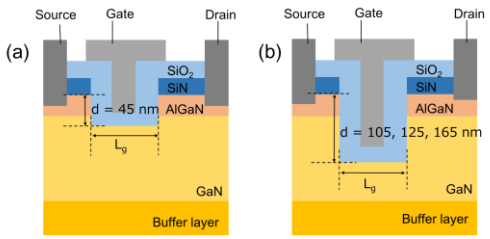

Fig. 2 Schematic image of recessed-gate GaN MOSFET. (a) Ref. (d = 45 nm). (b) Deep recessed-gate structure (d = 105, 125, 165 nm).

Thermal treatment of the etched GaN surface under NH_3 was carried out to remove ICP-RIE damage [8]. As a gate dielectric, a 30 nm-thick SiO_2 layer was deposited on the GaN layer by the ALD method. SiO_2 deposition was followed by post-deposition annealing to reduce electron traps in the gate dielectric [9]. The gate electrode metal TiN was deposited by the sputtering method. Finally, ohmic electrodes were formed as source and drain electrodes. The gate-source length and the gate-drain length were 6 and 14 μm, respectively.

4. Experimental Results and Discussions

Fig. 3 shows the bidirectional I_D-V_{GS} characteristics in semi-log scale at V_{DS} = 1 and 10 V for the recess depth of (a) Ref. (d = 45 nm) and (b) d = 165 nm. The negative V_{th} shift was observed in the case of Ref. of V_{DS} = 10 V. However, that could be effectively suppressed as shown in Fig. 3 (b) by means of deep recessed-gate structure. In addition, the leakage current of deep recess was almost the same as that of Ref.

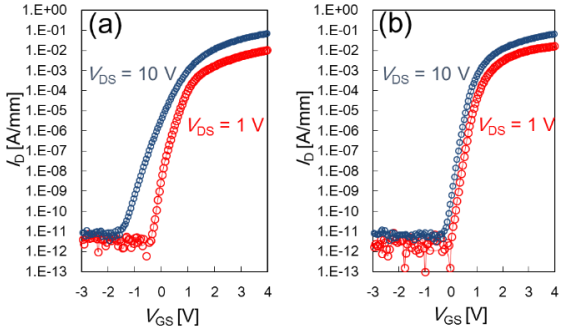

Fig. 3 Bidirectional I_D-V_{GS} characteristics in semi-log scale at L_g = 1 μm in (a) Ref. (d = 45 nm) and (b) Deep recessed-gate structure (d = 165 nm).

Fig. 4 shows the L_g dependence of V_{th}. Here, V_{th} indicates the V_{GS} at the drain current I_D of 1E-12 A and V_{DS} = 10 V. As shown in Fig. 4, the V_{th} roll-off is observed at the shorter L_g in the case of shallow recessed-gate. On the other hands, the V_{th} roll-off can be effectively suppressed in the deep recessed-gate structure.

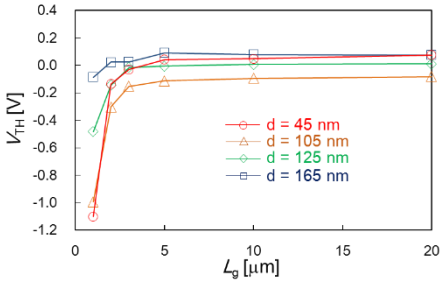

Fig. 4 L_g dependence of V_{th} shifts at the four recess depths.

Fig. 5 shows the bidirectional SS-V_{GS} characteristics at V_{DS} = 1 and 10 V in the case of the recess depth of (a) Ref. (d = 45 nm) and (b) d = 165 nm. SS degradation is confirmed in the case of Ref. of V_{GS} = 10 V. But, that cannot be observed in the deep recessed-gate structure. Moreover, the SS rise is almost the same V_{GS} = 1 and 10 V. The minimum SS indicates the good characteristics of SS = 90-100 mV/decade. Although the ICP-RIE damage may exist in the deep recessed-gate structure, it is shown that the SS degradation cannot be observed. That would be due to the thermal treatment of etched GaN surface under NH_3.

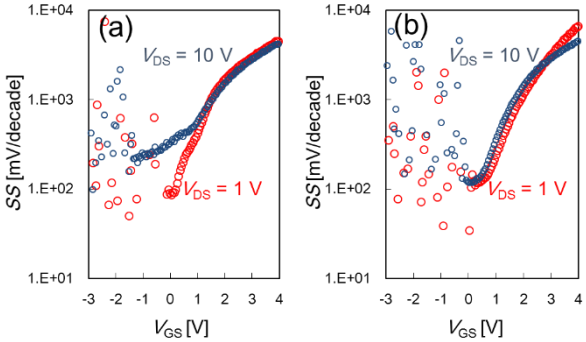

Fig. 5 Bidirectional subthreshold swing SS-V_{GS} characteristics at L_g = 1 μm in (a) Ref. (d = 45 nm) and (b) Deep recessed-gate structure (d = 165 nm).

Finally, we investigated the DIBL concerning the deep recessed-gate structure. Fig. 6 shows the dependence of the DIBL on L_g. As shown in Fig. 6, although DIBL is sharply increased in the case of the shallow recessed gate structure, this does not happen in the case of the recess depth of 165 nm.

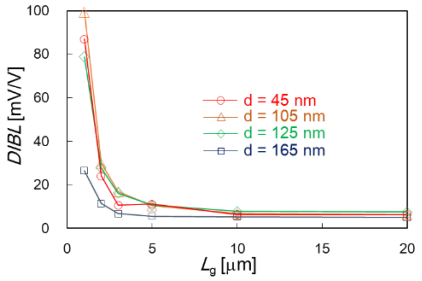

Fig. 6 L_g dependence of DIBL at the four recess depths.

5. Conclusions

The suppression of short-channel effects (SCEs) in normally-off GaN MOSFETs is demonstrated. The deep recessed-gate structure can reduce the electric field intensity around the recess edge. As a results, the characteristics of the negative V_{th} shift, the drain-induced barrier lowering and the subthreshold swing were improved by the fabricated devices with the recess depth of 165 nm. Since fabrication of the deep recessed-gate structure is simple, this structure is effective for suppressing SCEs in normally-off GaN MOSFETs.

References

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