K-1-04 Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp447-448

Vertical PN Junction-based GaN Power Diode

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Abstract

We demonstrated for the first time a completely horizontal pn diode featuring vertical-layered pn junction. The in-situ doping is achieved with a proprietary anisotropic epitaxial lateral overgrowth method. The pn diode demonstrates a breakdown voltage of 550V and specific on-resistance of 0.70 mΩ.cm^2 without further optimization of processing parameters. Such device geometry shows strong promise of delivering high performance and cost-effective diodes and transistors in the future.

1. Introduction

GaN has great promise for power electronics due to its wide bandgap, high critical electric field and high electron saturation velocity [1]. However, the commercialization of GaN-based power electronic devices is hampered by its high dislocation density and poor p-type doping effectiveness [2]. Epitaxial lateral overgrowth (ELOG) has been proved effective to grow GaN with ultra-low dislocation density in its overgrowth region (wing region) [3]. However, today's commonly-adopted device geometries, i.e., quasi-vertical (depicted in Fig.1(a)) and complete vertical (depicted in Fig.1(b)) could not bypass the high dislocation density region (window region) to withstand high blocking voltage.

Here we proposed novel device geometry: complete horizontal structure (depicted in Fig.1(c)), i.e., by switching pn junction from horizontal to vertical interface, the drift layer serving to block high voltage thus could overlap with the low-dislocation-density region of an ELOG GaN template.

In addition, the separate GaN islands can be naturally isolated from each other thus free of damages caused by mesa etch. Compared with Fig.1(a), the complete horizontal structure also helps eliminate the typical issue of current crowding in a quasi-vertical device. Such geometry also makes it convenient for the device to connect to outer circuit as both anode and cathode can easily access the pads without interfering with each other. The flexible layout facilitates further packaging and heat dissipation design, holding strong promise for success of commercialization in the future.

2. General Instructions

GaN Island Growth and Doping

In order to realize complete horizontal device geometry, the doping profile needs to be changed accordingly. Vertical-layered pn junction is adopted in lieu of conventionally-employed horizontal one, which is made possible by in-situ doping during lateral growth followed by dry etch to remove the top shell-like u/p+ GaN layers. For the lateral growth, we adopted a proprietary lateral growth method in which double layers of masks are used to create a serpentine channel so that most threading dislocations will glide out of the crystal during the grow through channel [4]. Fig.2 shows the SEM image of an array of as-grown GaN islands which grows out of the window of upper mask.

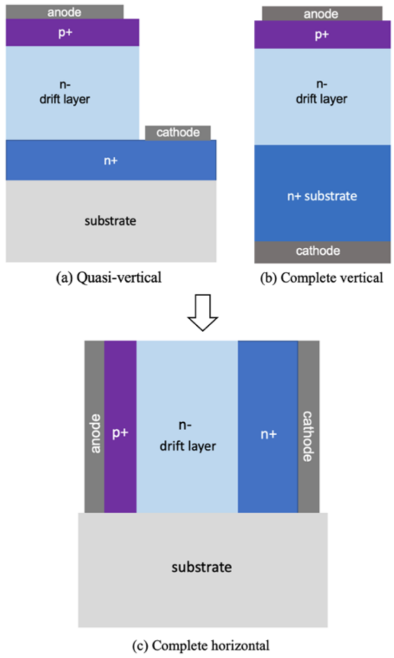

Fig.1 Cross-sectional schematic comparison between (a) conventional quasi-vertical, (b) complete vertical and (c) complete horizontal device structure.

Device Fabrication

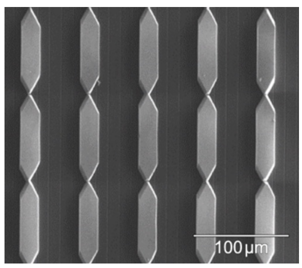

Fig. 2 The plan-view of an array of as-grown GaN islands.

Fig.3(a) depicts the designed pads layout and separate pn diodes. Compared with Fig.2, half of each island was etched off in order to expose the n+ sidewall for cathode deposition. As shown in Fig.3(c), Ti/Al/Ni/Au was deposited onto the vertical sidewall of the half island serving as ohmic contact to n$^+$-

GaN. In the same manner, Ni/Au was deposited onto another side of the island serving as ohmic contact to p$^+$-GaN. Both anode and cathode can be easily connected to the outer circuit due to its special layout, making it convenient for packag ing with enhanced heat dissipation efficiency.

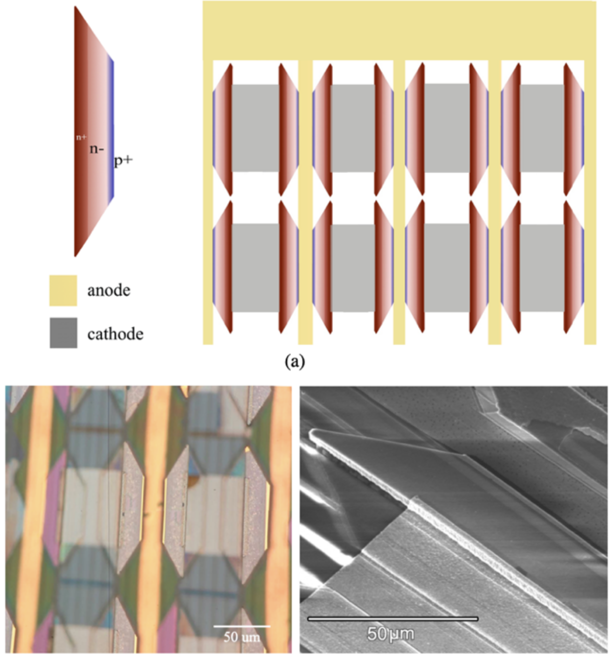

Fig. 3 (a) Plan-view schematics of pn diodes and contact pad layout; (b) Optical microscopic image of as-fabricated diodes; (c) The angled-view SEM image showing the cathode was deposited onto the vertical island sidewall.

Device Characterization

Fig.4(a) shows the forward bias I-V characteristic curve. The specific on-resistance is measured to be 0.70 mΩ.cm^2. In order to suppress leakage in the reverse bias, the diodes were passivated using a thin insulating layer of A_2O_3 (30nm). Al_2O_3 was deposited on the entire sample by atomic layer deposition (ALD). Fig.4(b) shows the reverse bias I-V curve until breakdown occurs. The breakdown voltage is 550V. The doping concentration of the drift layer is 3×10^{16} cm^{-3}. An approximate breakdown field of 2.54 MV.cm^{-1} is obtained. The ideality factor is 4.7 which lies in the range of ideality factors (2-7) typically observed in GaN p-n diodes [5][6].

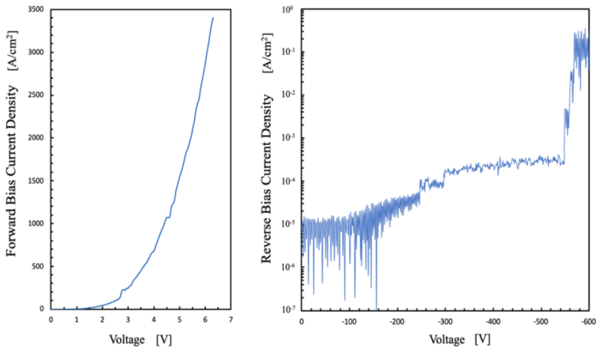

Fig. 4 (a) Forward and (b) reverse bias characteristics of pn diode.

To draw comparison with some state-of-the-art GaN pn diodes, this work is benchmarked with other recent works in the literature, as shown in Fig.5. It could be seen that the performance is comparable to the best GaN pn diodes on foreign substrate. It is worth mentioning that the optimization of processing parameters in our future work should further enhance breakdown voltage and reduce specific on-resistance.

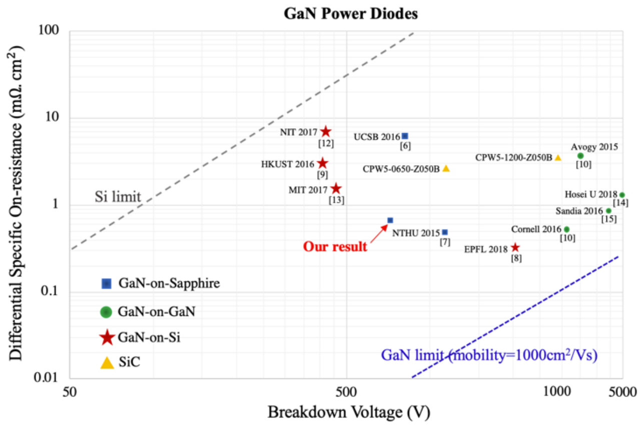

Fig. 5 Comparison of this work with other recent works in the literature [6-15].

3. Conclusions

GaN pn diode with complete horizontal geometry is proposed and demonstrated for the first time. The structure features numerous advantages that are otherwise unattainable. The breakdown voltage and specific on-resistance are among those of the state-of-the-art GaN diodes on foreign substrate. The optimization of processing flow and parameters should further enhance the device performance. Complete horizontal structure hence holds strong promise of delivering high-performance diodes and transistors in the future.

Acknowledgements

We would like to express sincere thanks to the programs of NUPACE (Nagoya University Program for Academic Exchange) and JUACEP (Japan-US Advanced Collaborative Education Program) as bridges which lead to this collaborative research work.

References

[1] H. Amano *et al*., J. Phys. D: Appl. Phys. **51** (2018) 163001.
[2] K. Shenai *et al*., IEEE Trans. Electron Devices **62** (2015) 248.
[3] A. Usui *et al*., Jpn. J. Appl. Phys. **36** (1997) L899.
[4] L. Li *et al*., App. Phys. Express **5** (2012) 051001.
[5] V. A. Dmitriev, MRS Internet J. Nitride Semicond. Res. **29** (1996).
[6] C. Gupta *et al*., Phys. Status Solidi A **213** (2016) 878.
[7] B. Zheng *et al*., IEEE Electron Device Lett. **36** (2015) 932.
[8] R. A. Khadar *et al*., IEEE Electron Device Lett. **39** (2018) 401.
[9] X. Zou *et al*., IEEE Electron Device Lett. **37** (2016) 636.
[10] I. C. Kizilyalli *et al*., IEEE Trans. Electron Devices **62** (2015) 414.
[11] K. Nomoto *et al*., IEEE Electron Device Lett. **37** (2016) 161.
[12] S. Mase *et al*., IEEE Electron Device Lett. **38** (2017) 1720.
[13] Y. Zhang *et al*., IEEE Electron Device Lett. **38** (2017) 248.
[14] H. Ohta *et al*., Jpn. J. Appl. Phys. **57** (2018) 04FG09.
[15] A. M. Armstrong *et al*., Electronics Letters **52** (2016) 1170.