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State-of-the Art IGBT and Development towards Higher Operation Temperature and Power Ratings

J. Vobecky, C. Corvasce, E. Buitrago, M. Andenna, B. Boksteen, G. Paques

ABB Semiconductors
Fabrikstrasse 3, Lenzburg
5600 Switzerland
Phone: +41-58-586-1769 E-mail: jan.vobecky@ch.abb.com

Abstract

A recent progress of the classical silicon IGBT – diode concept and the advanced reverse conducting concept BiGT is discussed. The focus is laid on the design leading to increased maximal junction temperature, reduced energy losses and increased power density of power modules.

1. Introduction

Further innovations of the IGBT concept are coming to light despite more than 30 years of its development [1]. The main reasons are a very good performance/cost ratio of the IGBT modules for the medium and high-power applications from kilowatts to gigawatts, controllability of turn-on and turn-off via the MOS input, capability to survive fault cases without bulky solutions as well as still improving reliability. This motivates us to push further the limits of this device concept.

The development efforts concern both the MOS transistor cell and vertical structure as the only way to satisfy the complex demands laid on today`s IGBT. A special focus is also put on the thin wafer technology and dopant activation important for the mainstream low voltage classes 450-1700 V.

A further increase of the converter output current for a given voltage level is possible thanks to the reduced energy losses, increased maximal junction temperature and increased power density using the BiGT. These topics are discussed and completed by some relevant packaging concepts.

2. IGBT Development Trends

MOS Transistor Cell

Fig.1 shows the evolution of MOS cell design for the HV IGBT and its benefit for the rating current of HiPak modules from ABB [2]. For the LV IGBTs, the choice of the cell concept is more aggressive. There have recently emerged new concepts like the micro pattern trench [4], side gate [5] and narrow mesa [6] to further reduce the V_{cesat} by increasing the plasma concentration at the MOS side. The widely spread trench concept is further mastered by shielding the trenches to reduce the Miller capacitance [7], by adding the source trenches and dummy gates to balance C_{gd} and C_{gs} [8] and to protect the bottom part of the MOS cell from high electrical fields during hard switching (dynamic avalanche) to avoid switching instability resulting from the injection of hot carriers into the oxide layer [9].

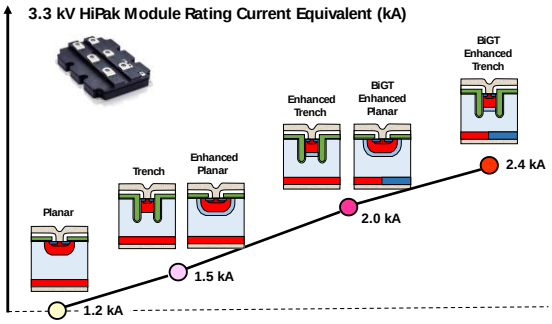

Fig. 1 MOS cell evolution of HV IGBT. *Enhanced* = enhancement of carrier concentration at bottom of P-well or trench [3].

Vertical Structure and Thin Wafer Concept

The state-of-the-art IGBTs utilize the punch-through (PT) concept with lightly doped n-type anode buffer called Field Stop [10] or Soft Punch-Through [11]. When the wafer thickness is chosen with the PT voltage more than 70% of the breakdown voltage, we receive the Maximum Punch-Through (MPT) design with a minimal silicon consumption by the buffer itself [12]. The importance of the concepts above consists not only in minimizing the wafer thickness for the lowest losses, while keeping the same breakdown voltage. It also introduces a possibility to achieve at the same time a low leakage current, high maximal junction temperature, low losses (either low V_{cesat} or E_{off}), high short circuit current capability, high RB SOA, and soft switching.

While the IGBT wafer thickness and n-drift resistivity gradually reached the MPT design (the lowest thickness and maximal resistivity for given breakdown voltage), further development has focused on the thin wafer process [13], where the buffer design plays a prominent role (Fig.2). At the low-voltage IGBT, the original corpulent SPT buffer had shrunk (LV SPT) within the wafer grinding process. Later on, one more phosphorus peak has been added to lower the leakage current (CPT, APT) [14, 15]. Eventually, the laser annealed MPT phosphorus buffer (top right) was replicated using the substrate of a wafer with an epi-layer. Except for the CPT concept, these buffers use the classical dopants like boron and phosphorus (also in pre-diffused wafers) and activation during metal sintering and/or by laser annealing.

The limited processing temperature after completion of the MOS part and wafer thinning stimulated the replication of the SPT buffer (bottom left) [16] using proton implantation

and annealing below 500 °C. The combination of proton and phosphorus implantation enabled us to shrink the buffer to its absolute minimum and bring the thickness of the 1200 V IGBT to its theoretical limit of ≈100 µm (CPT) [14]. Later on, the idea of the triple hydrogen buffer (bottom right) without phosphorus peak has been introduced commercially [8].

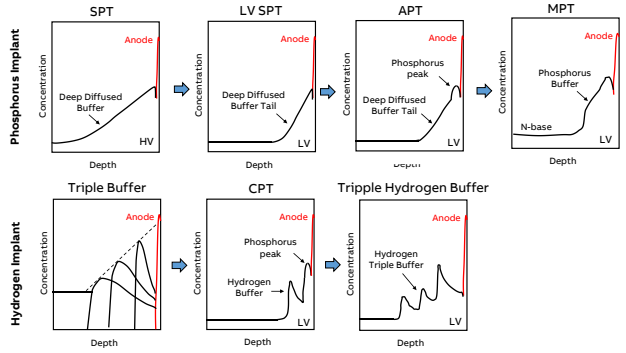

Fig. 2 Anode buffer evolution IGBTs using classical dopants (top) and hydrogen thermal donors (bottom).

Towards High Temperature Operation

The latest investigations suggest that the only stable buffers under 200 °C operation of the LV IGBTs are the ones with classical dopants showing the leakage current <10 mA at 200 °C at the same time having a minimal buffer thickness like the MPT above [15, 17]. The thin CPT buffer, with only one peak using the hydrogen-related shallow donors (HD), also shows a low leakage current <10 mA, but it still suffers from thermal run away over time at 200 °C. A suitable vehicle for analysis of potential reasons can be a diode test structure with a well activated boron anode (Fig.3 left). The hydrogen-related part of the CPT buffer can be then characterized through the profiles of carriers received from the SRP and C-V measurements. The DLTS method can be used to compare the amount of defects between a diode with and without the hydrogen buffer to identify the rest of radiation defects responsible for a lower thermal stability (Fig.3 right).

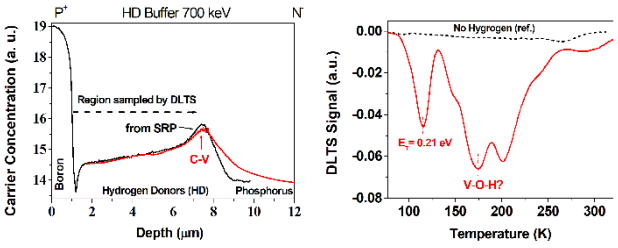

Fig. 3: Spreading Resistance (SRP) and C-V measurement at the anode side of a diode with the HD (left) and DLTS spectrum after annealing of CPT buffer (red) and reference diode (black).

Towards Higher Power Density

Power density has been increased using a device concept BiGT [19], which integrates an RC-IGBT and an IGBT in a single chip to satisfy the design and performance trade-off challenges. The first HV BIGTs were employed in a state-of-the-art Stakpak housing and optimized for an HVDC breaker. For the latest VSI based HVDC systems, the BIGT was combined with a new Stakpak housing for current ratings up to 3 kA. Both the BiGT and the Stakpak were optimized for an HVDC converter using the MMC concept (low switching frequency and asymmetric loading in diode/IGBT mode).

3. Diodes

High voltage fast recovery diode concepts for high temperature operation are the EMCON without and the FSA with the local lifetime control [19]. For a sufficiently high RB SOA an optimized junction termination (JT) with resistive zone between the JT and active region is a must. This provides reliable 3.3 - 6.5 kV products up to 150 °C and 1.7 kV ones up to 175 °C [20].

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