Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp453-454

Impact of Structural Parameter Scaling on On-state Voltage in 1200V Scaled IGBTs

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Abstract

The effect of structural parameter scaling on 1200V IGBT was systematically investigated in both non-scaled (*k*=1) and scaled (*k*=3) IGBTs, and clear on-state voltage improvement was verified in scaled IGBTs. The origin of the performance improvement is discussed

1. Introduction

While many power devices with new wide bandgap materials are developed, Si-IGBTs (Insulated Gate Bipolar Transistors) are still making steady progress [1]. In the previous study, we have demonstrated both improved on-stage voltage (V_{cesat}) and reduced turn-off loss (E_{off}) in 1200V-10A IGBTs [2] based on the scaling concept of Si-IGBTs (Fig.1) [3,4]. Similarly to the CMOS scaling, all the geometrical dimensions as well as gate voltage are scaled down proportionately while keeping the cell pitch *W* constant. The improved V_{cesat} vs E_{off} trade-off has also been verified in 5V-drivien 3300V-4A scaled IGBTs [5]. In these studies, the area of fabricated chips was large enough to attain 10A or 4A class on-current (active emitter area: 5mm^2), and the structural parameters were fixed in both non-scaled and scaled IGBTs, respectively. Details of the effects of structural parameters remained unclear and the intrinsic origin of improved performance should be clarified.

In this study, we fabricated relatively smaller size IGBTs with varied device parameters and evaluated V_{cesat} systematically. Superior characteristics in scaled IGBTs were demonstrated and its origin was discussed from the measured data of the parameter dependence.

2. Device Design and Fabrication

Table 1 shows parameters of fabricated 1200V IGBTs, where *k* is the scaling factor. The *k*=1 device is the conventional non-scaled IGBT. The *k*=3 device is the fully scaled IGBT (except for cell pitch *W*). The $k=1^+$ is basically *k*=1 but the mesa width (*S*) is scaled, while $k=3^-$ is basically *k*=3 but *S* is not scaled. Figs. 2 and 3 show photos of fabricated wafer and device, respectively. The fabricated device is included in a TEG chip and has identical structure to an IGBT chip with *W* of 16μm and trench length of 1mm, except that the present device consists of only 9 pairs of trench gates (active emitter area: 0.14mm^2) and the p-float is not connect to the ground. Table 2 summarizes parameters of all devices. 12 types of devices were fabricated in total.

Figs. 4 and 5 show simulated $I_{ce} - V_{ce}$ characteristics and carrier distribution for *k*=1 and *k*=3 devices. It is confirmed that, in the *k*=3 device, the front side carrier concentration is selectively increased by the injection enhancement (IE) effect [6] and the ideal flat carrier concentration is realized, leading to reduced V_{cesat}.

3. Device Characteristics

Fig.6 shows measured $I_{ce} - V_{ce}$ characteristics of all devices. The *k*=1 group (A~F) and the *k*=3 group (G~L) respectively show almost identical curves irrespective of mesa width *S* and p-collector dose. Figs. 7 and 8 show measured threshold voltage (V_{th}) and subthreshold factor (*S.S.*). Thanks to scaled gate oxide thickness (33nm) in *k*=3, reduced V_{th} variability and improved *S.S.* were observed.

Measured and simulated $I_{ce} - V_{ce}$ are compared in standard *k*=1 and *k*=3 (B and K) in Fig. 9. Both are in good agreement. Reduced V_{cesat} (at J_{ce}=200A/cm^2) in *k*=3 is confirmed. This improvement is larger than that in a large area IGBT chip in [2]. This is because the p-float is not connected in the present device resulting in enhanced IE effect while the p-float is grounded in an IGBT chip for stable switching operations [2]. The dependences on back side p-collector dose are shown in Fig. 10. It is found that V_{cesat} improves with p-collector dose more in *k*=3 than *k*=1.

Measured average V_{cesat} and on-current (at V_{ce}=1.25V) are summarized in Fig.11. It is found by comparing the differences in $k=1/k=1^+$ and $k=3^-/k=3$ that the sensitivity to *S* is larger in *k*=3 than in *k*=1. It is also confirmed that the sensitivity to p-collector dose is also larger in *k*=3 than *k*=1. These results suggest that the IE effect (and hence V_{cesat}) is saturating with decreasing *S* in conventional non-scaled IGBTs. On the other hand, there is more room in V_{cesat} improvement with *S* scaling in *k*=3. Moreover, although the E_{off} degradation should be considered, further V_{cesat} improvement is expected in *k*=3 by the increase in the p-collector dose because of the front side carrier concentration enhancement due to the IE effect.

4. Conclusions

The structural parameter dependence in IGBT is investigated in order to explore the possibility of further improvement by scaling. It is shown that the scaled IGBT has more room for improvement by parameter optimization than the conventional non-scaled IGBT.

Acknowledgements

The authors would like to thank Dr. K. Satoh of Mitsubishi Electric Corp., Dr. T. Matsudai of Toshiba Electronic Devices & Storage Corp., Dr. M. Tsukuda of Green Electronics Research Institute, and Prof. W. Saito of Kyushu University for fruitful discussions. This work is based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

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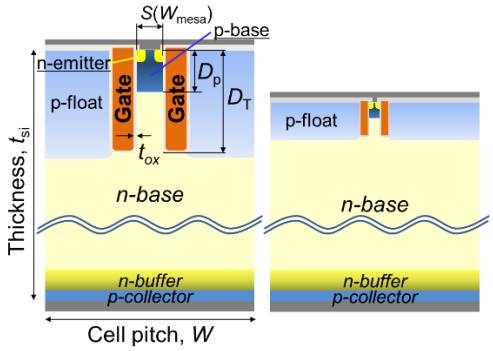

(a) k=1 (b) k=3

Fig. 1. Scaling principle of trench gate IGBTs.

Table 1. Structural parameters of scaled IGBTs.

	k=1	k=1⁺	k=3⁻	k=3
Cell pitch, W	1	1	1	1
Mesa width, S	1	1/3	1	1/3
Trench depth, D_T	1	1	1/3	1/3
p-base depth, D_P	1	1	1/3	1/3
Trench extrusion, D_T - D_P	1	1	1/3	1/3
Gate oxide thickness, t_{ox}	1	1	1/3	1/3
Gate voltage, V_g	1	1	1/3	1/3

Table 2. Sample classification by scaling factor and p-collector dose.

	p-collector dose		
	x1/2	X1 (typ.)	x2
k=1	A	B	C
k=1⁺	D	E	F
k=3⁻	G	H	I
k=3	J	K	L

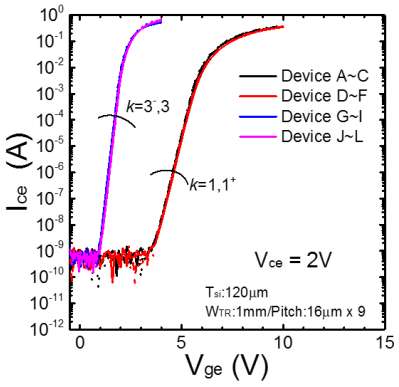

Fig. 6. I_{ce} – V_{ge} characteristics of 1200V k=1 and k=3 IGBTs.

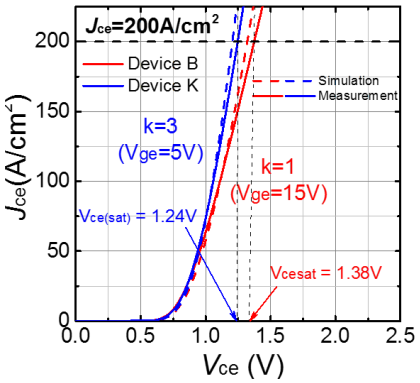

Fig. 9. I_{ce} (J_{ce}) – V_{ce} characteristics of 1200V k=1 and k=3 IGBTs.

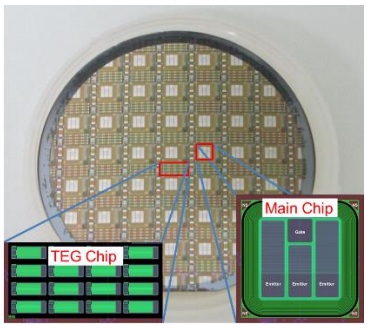

Fig. 2. Chip photograph of IGBT wafer fabricated in facilities of the Univ. of Tokyo.

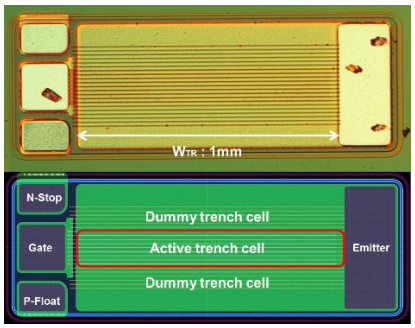

Fig. 3. Photograph and layout of TEG chip

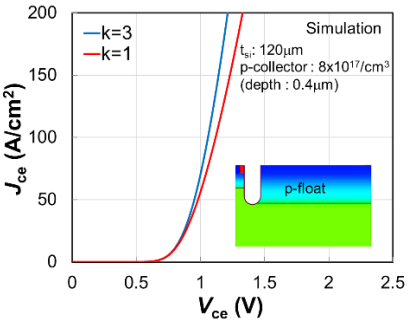

Fig. 4. Simulated on-state characteristics of k=1 and k=3 trench gate IGBTs.

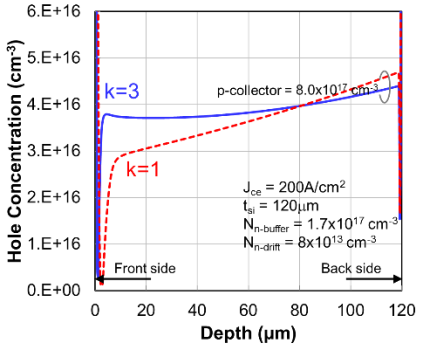

Fig. 5. Simulated carrier distribution on k=1 and k=3 IGBTs.

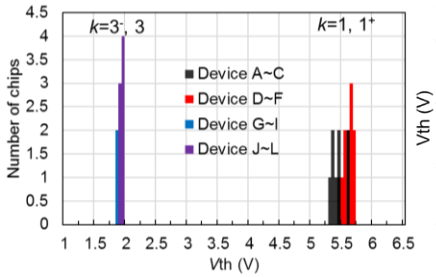

Fig. 7. Threshold voltage distribution of k=1 and k=3 IGBTs.

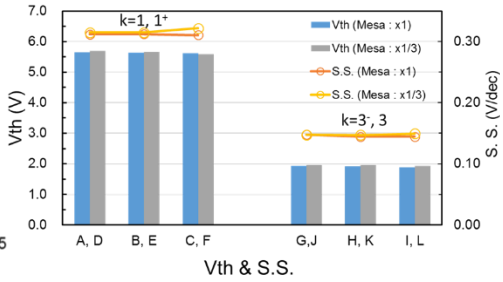

Fig. 8. Comparison of average threshold voltage and subthreshold slope of k=1 and k=3 IGBTs for different mesa width.

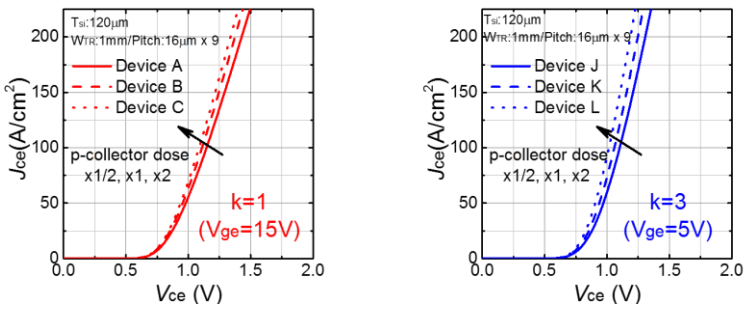

Fig. 10. The p-collector dose dependence of I_{ce} (J_{ce}) – V_{ce} characteristics of k=1 and k=3 IGBTs.

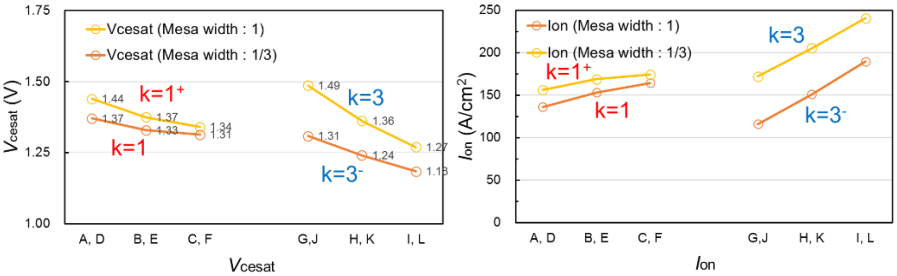

Fig. 11. Comparison of on-state voltage and on-current of k=1 and k=3 IGBTs for different mesa width.