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Practical Extraction Method of Interface State Density near Conduction Band Edge of 4H-SiC MOSFET Channel

Shintaroh Sato[1], Keisuke Kobayashi[1], Yuki Mori[1], Digh Hisamoto[1] and Akio Shima[1]

Research & Development Group, Hitachi Ltd.,
Higashi-Koigakubo 1-280, Kokubunji-shi, Tokyo 185-8601, Japan
Phone: +81-42-323-1111 E-mail: shitaroh.sato.hn@hitachi.com

Abstract

We proposed a simple method to evaluate interface state density (D_{it}) near conduction band edge of 4H-SiC MOSFETs, which was difficult to observe by conventional method although they degraded device characteristics. We focus on capacitance-voltage method with inversion capacitance applying high voltage to set reference point where almost of all trap were occupied and sweeping downward gradually. Our method is applicable for mass-production because of the convenient sequence. We also demonstrated that the device characteristics calculated based on the extracted D_{it} were in good agreement with the measured characteristics.

1. Introduction

Silicon carbide (SiC) metal-oxide-semiconductor field effect transistor (MOSFETs) has been recognized as next generation power devices and circuit elements that can be used in high temperature harsh environment. However, it still has suffered from large interface trap density of state, D_{it}.

Conventionally, capacitance-voltage (*C-V*) method and conductance method have been used to measure D_{it} with accumulation capacitance [1-3]. The measurable energy range was 0.2-0.6 eV whereas shallower traps would be dominant to on-state characteristics of SiC-MOSFET.

The recent progress with Hall measurement had made it possible to evaluate such shallow traps [4,5]. These methods have been used to estimate fundamental properties of SiO_2/SiC interface [6,7]. Because Hall measurement is not suitable for wafer-level testing in mass-production, the development of the simple measurement is required.

In this paper, we focused on the difference between the shallow and deep trap. Generally, shallow traps are originated physical properties of SiC, e.g., atomic staking configuration [8], carbon-related defects [9], and affect the inversion layer characteristics. However, it appears superficially that deep traps only cause hysteresis phenomenon due to the long time constant. Therefore, shallow traps would be easily measurable once we obtain correct *C-V* curve. By using proper *C-V* characteristics, we demonstrate that the shallow interface traps of 4H-SiC MOSFETs can be evaluated quantitatively.

2. Fabrication and experimental method

Lateral n-channel SiC-MOSFET was fabricated by following process. P-well region were formed by ion implantation, $N_a = 4 \times 10^{17}$ cm^{-3}, on n-type 4H-SiC (0001) substrate. Then, p-type and n-type contact region were formed. Acceptor and donner ion were Al and N, respectively. They received 50-nm-thick gate oxide deposited by chemical vapor deposition. Post-Oxidation-Anneal was conducted in a nitric oxide containing atmosphere. The phosphorus-doped n-type gate poly-Si was deposited and patterned. Electric contact to substrate and metal electrode was formed. Channel length and width were 100 μm and 200 μm, respectively.

We measured *C-V* curve with quasi-static method, QSCV, and I_d-V_g characteristics (V_d = 50 mV). Keysight B1500A and 4156C were used, respectively. The gate voltage was swept from +20 V to −20 V. For V_g = +20 V, MOSFET is in on-state so that the conduction band edge of SiC approaches the Fermi level. Therefore, the evaluated energy range was so low between about 0.05 eV to 0.2 eV.

It is worth pointing out that QSCV measurement results depended on *initial negative voltage* when the gate voltage was swept upward. When the intrinsic level exceeded Fermi level, mid gap donor-like interface states with long time constant were positive. Therefore, we could eliminate the hysteresis by applying high voltage and by sweeping downward gradually.

The theoretical *C-V* curve was calculated by [10]

$$C_s(\psi_s) = \frac{dQ_s(\psi_s)}{d\psi_s} \quad (1)$$

$$C_g(\psi_s) = \frac{C_{ox}C_s(\psi_s)}{C_{ox} + C_s(\psi_s)} \quad (2)$$

$$V_g = \psi_s + \varphi_{MS} - \frac{Q_s(\psi_s) + Q_{ox}}{C_{ox}} \quad (3)$$

where C_s is SiC capacitance per area, ψ_s is surface potential, C_g is gate capacitance of MOSFET per area, C_{ox} is gate oxide capacitance per area, V_g is gate voltage, φ_{MS} is work function difference between poly-Si and SiC and Q_{ox} is equivalent oxide charge.

To calculate D_{it}, ψ_s was estimated from QSCV result, C_{QS}, using [11]

$$\psi_s(V_g) = \int \left(1 - \frac{C_{QS}(V_g)}{C_{ox}}\right) dV_g + A \quad (4)$$

where A is an integral constant. D_{it} was given by [15]

$$D_{it} = \frac{C_{QS} - C_s}{q^2}. \quad (5)$$

The number of total trapped electrons per unit area by interface trap, N_{tot}, was estimated by

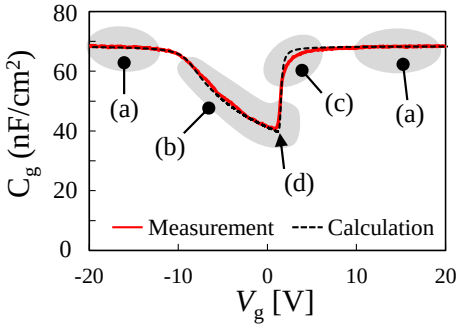

Fig. 1 *C-V* characteristics of n-channel MOSFET.

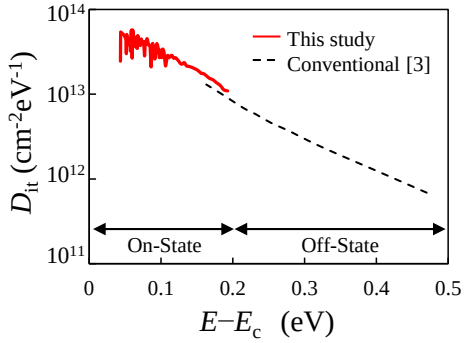

Fig. 2 D_{it} distribution calculated by *C-V* method with inversion capacitance of n-channel MOSFET.

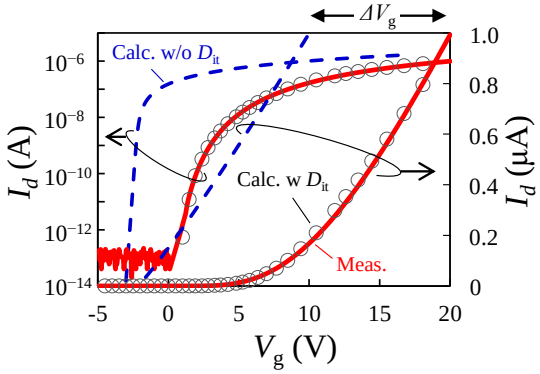

Fig. 3 Measurement and calculation result of I_d-V_g.

$$N_{\mathrm{tot}} = \int_{E_i}^{E_c} D_{\mathrm{it}}(E)\, f(E,T)\, dE \qquad (6)$$

where E_i is intrinsic Fermi level, E_c is conduction band energy and f is Fermi-Dirac distribution. The gate-voltage-shift, ΔV_g, due to N_{tot} was calculated by

$$\Delta V_g = \frac{qN_{\mathrm{tot}}}{C_{\mathrm{ox}}}. \qquad (7)$$

I_d-V_g characteristics was calculated by Pao & Sah Double Integral (PSDI) with D_{it} that we reported in Ref [12].

3. Results

Figure 1 plots the measurement result of QSCV and the calculation result. In the region labeled (a), the measurement results were exclusively fitted by C_{ox}. In the region (b), we could fit the slope by theoretical result with two fitting parameters, N_a and Q_{ox}. If the gate voltage swept upward in this region, hysteresis prevented us from fitting and obtaining those parameters. In addition, our method can utilize the inversion point labeled (d) so that we can easily evaluate those parameters with higher accuracy. Extracted parameters were $C_{ox} = 6.80 \times 10^{-8}$ F/cm^2 (gate oxide thickness, $t_{ox} = 49.5$ nm), $N_a = 4.00 \times 10^{17}$ cm^3 and $Q_{ox}/q = 3.10 \times 10^{12}$ cm^2.

In the region labeled (c), measured *C-V* curve was broadened in the positive direction because the negative trapped charges due to the interface trap states shifted the gate voltage. We calculated D_{it} by these difference between measurement and calculation results with eq. (4) and (5)

Figure 2 shows the D_{it} distribution. We could measure shallower interface traps density than conventional method. It was in the order of ten to the thirteen. According to eq. (6), total trapped charge at $V_g = 20$ V was estimated, $N_{tot} = 4.9 \times 10^{12}$ cm^{-2}. We also estimated the gate voltage shift with eq (7), $\Delta V_g = 11.5$ V. This indicate that such huge gate voltage shift occurred over inversion point.

Figure 3 showed I_d-V_g characteristics. The calculation results with shallow interface traps (black circle) was consistent with measurement results (red solid line) in both liner and log plot. It indicates the validity of our method.

The calculation result without interface traps was also plotted (blue broken line). For $V_g > V_{th}$, almost of all traps were occupied so that the gate-voltage-shift is consistent to that we had expected by *C-V* measurement, $\Delta V_g = 11.5$ V. For subthreshold region, only deep interface traps were occupied, and the gate voltage decreased by about 3 V.

4. Conclusions

We estimate interface trap density by QSCV measurement with n-channel SiC-MOSFET. To sweep V_g downward from high voltage avoid hysteresis effect due to mid gap state and gave us the distribution of the shallow traps in 0.2 eV energy depth from conduction band edge, which was in the order of ten to the thirteen. We demonstrated that this huge amount interface traps caused the gate over drive voltage degradation in I_d-V_g characteristics. Because the proposed method is so simple that it can be used for wafer-level testing in mass-production, it will open up new opportunities to improve the device performance and circuits operation.

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